

FIG. 1 PRIOR ART

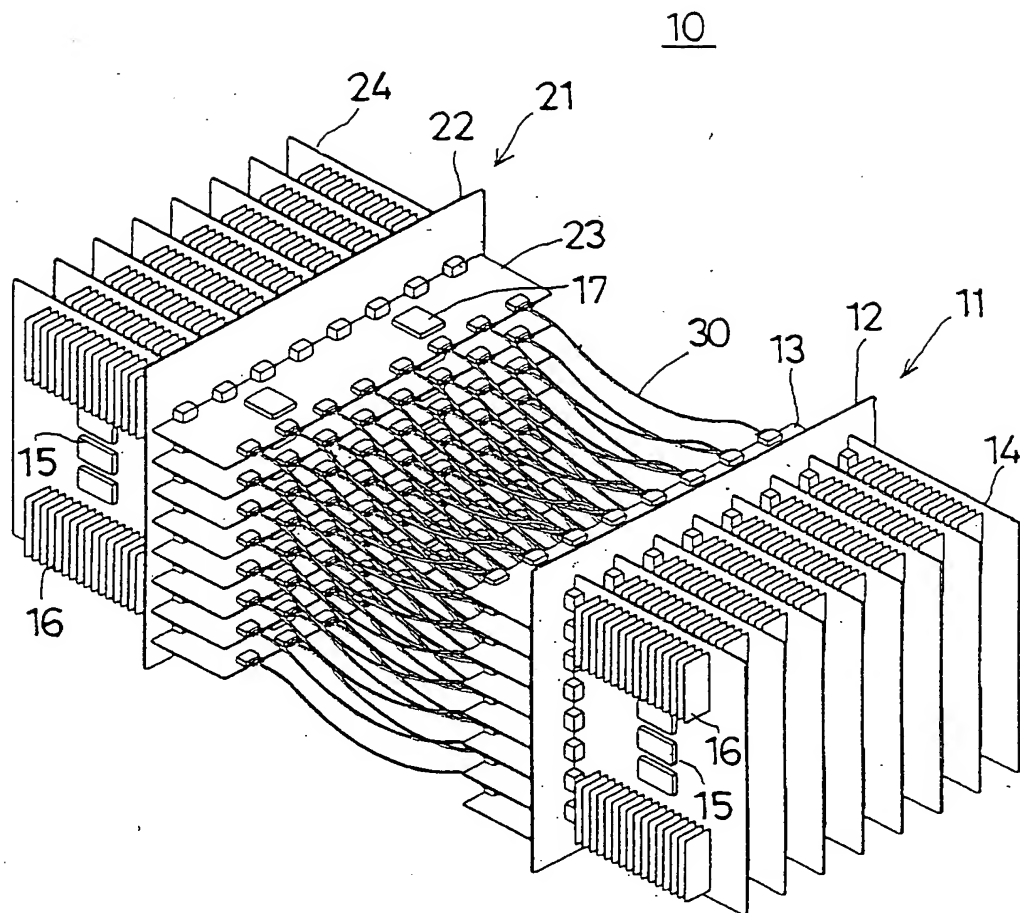


FIG. 2

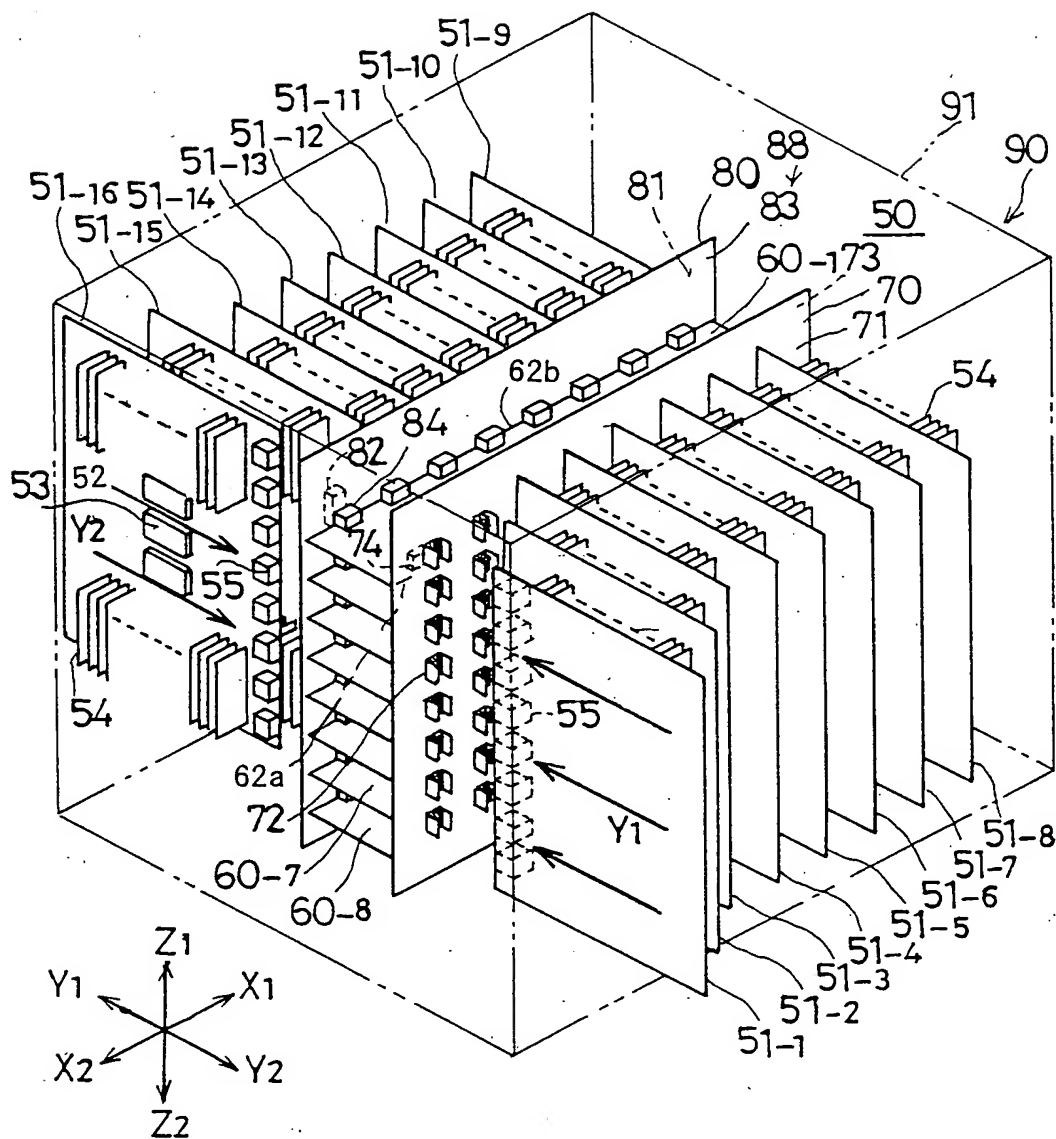


FIG. 3

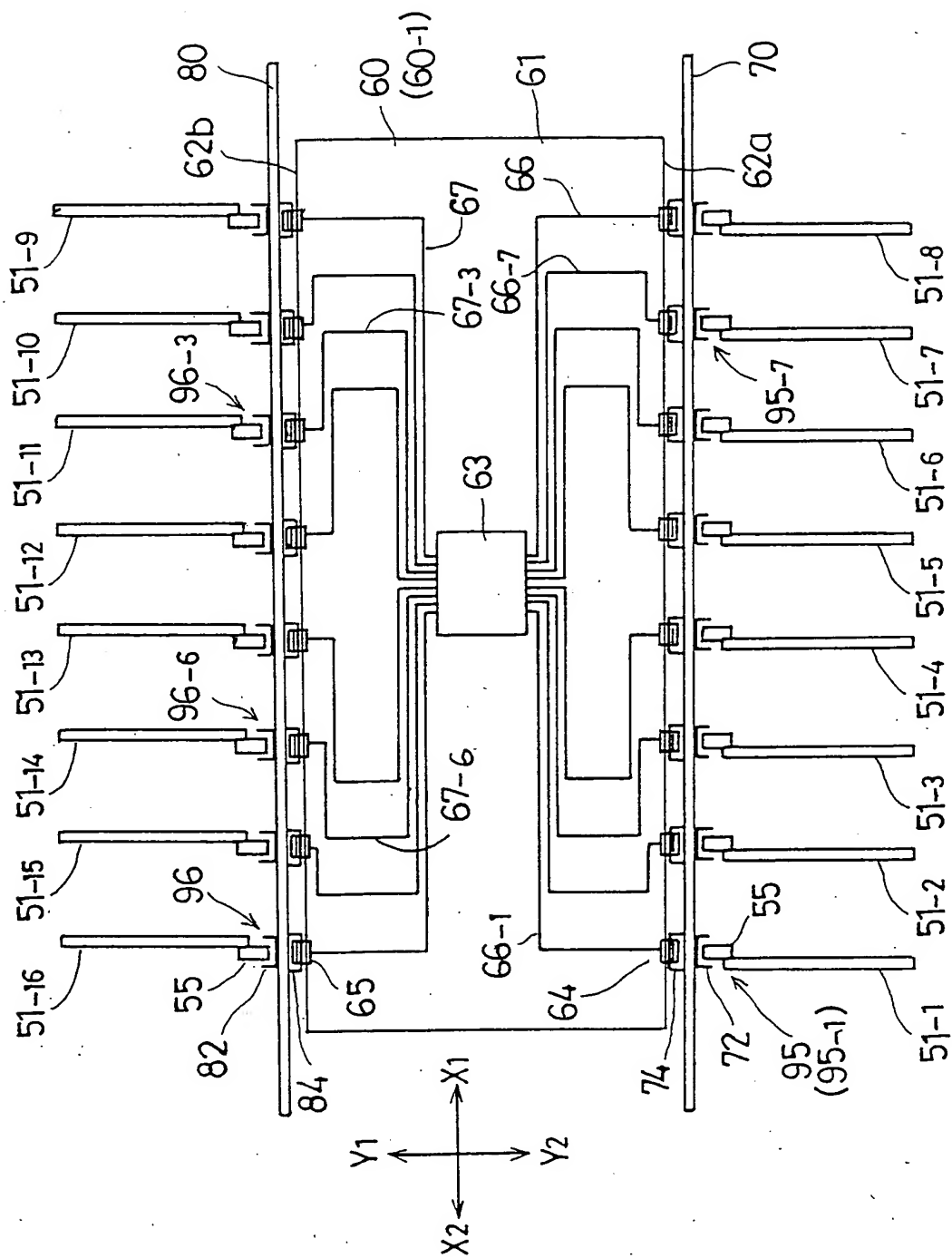


FIG. 4

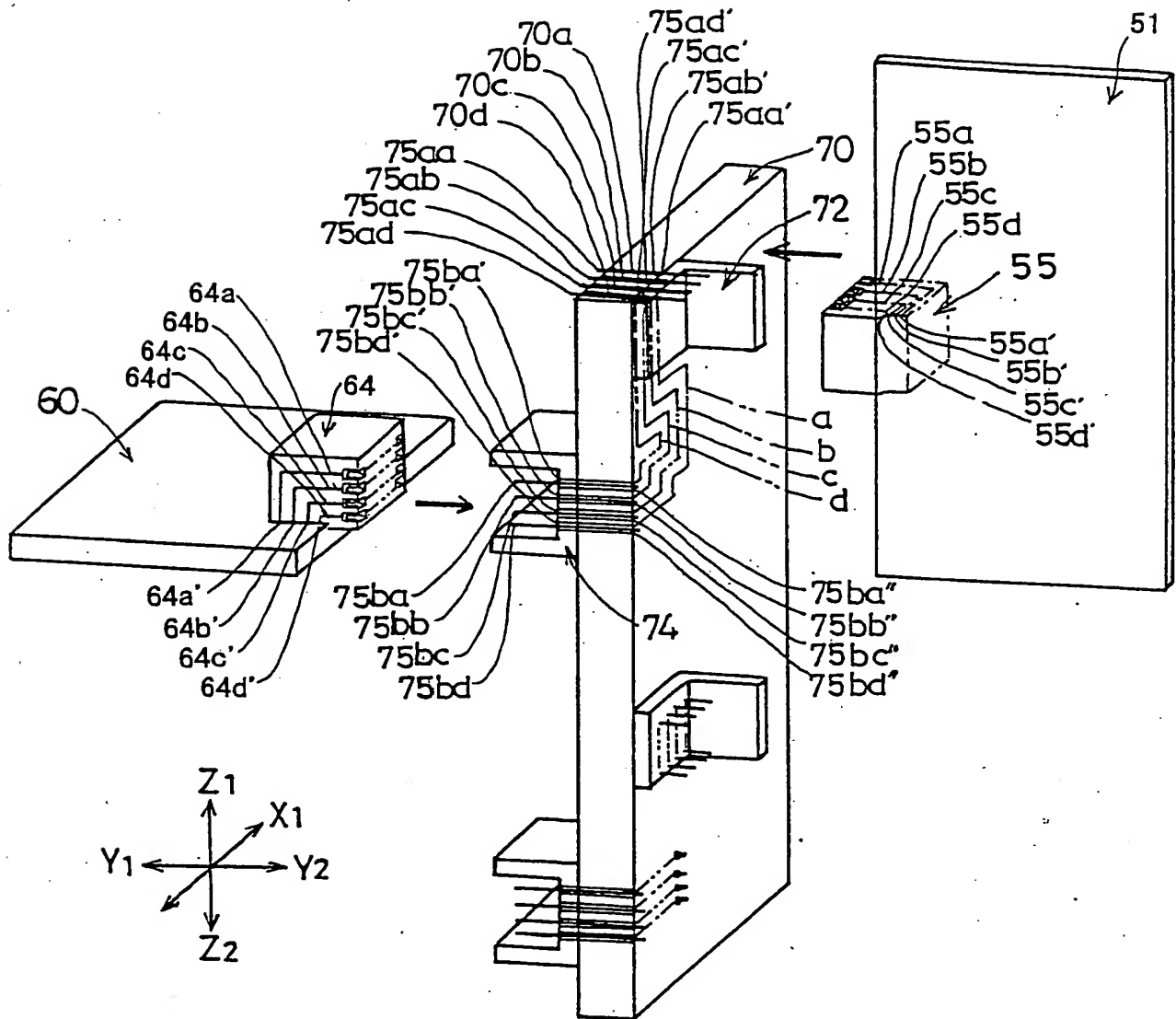


FIG. 5

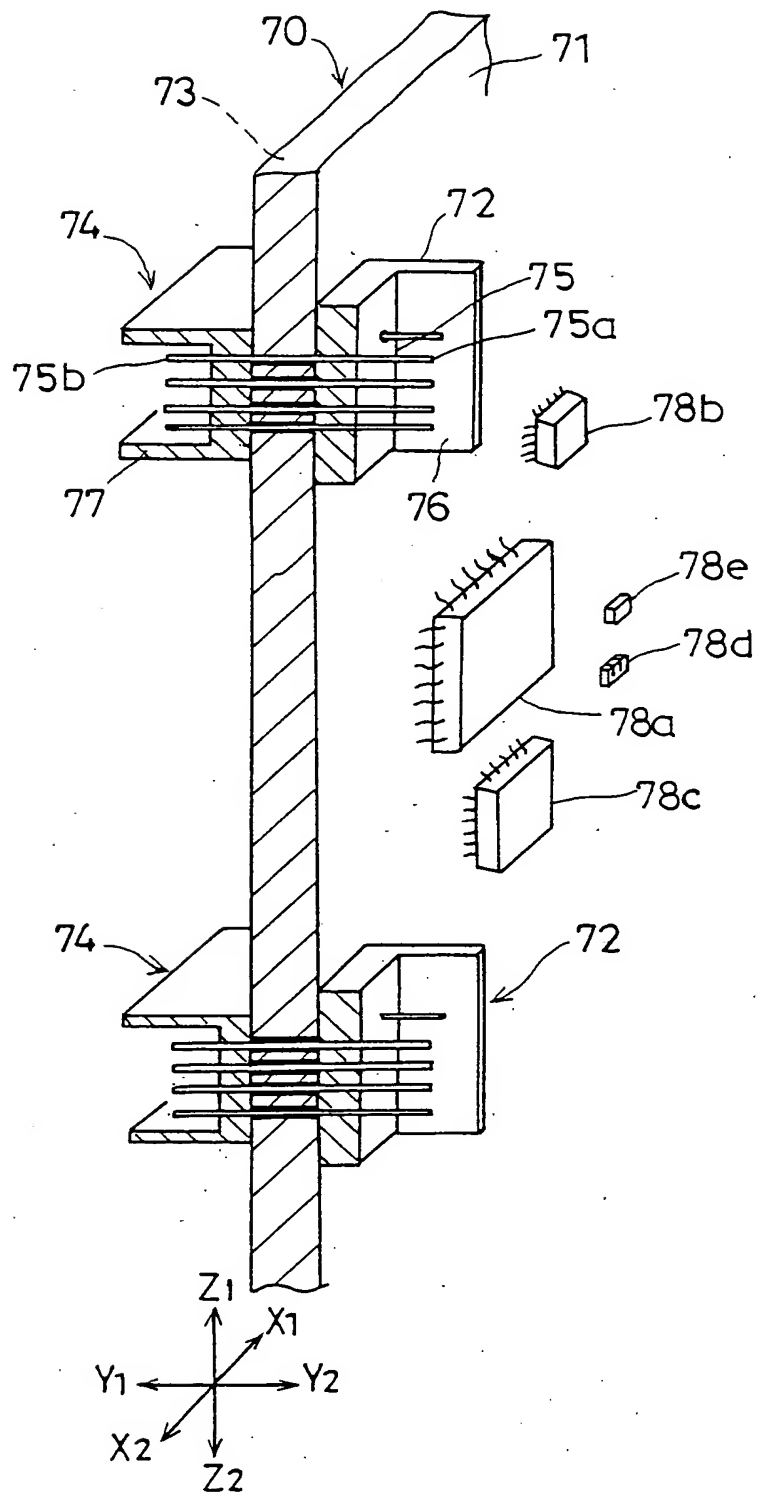


FIG. 6

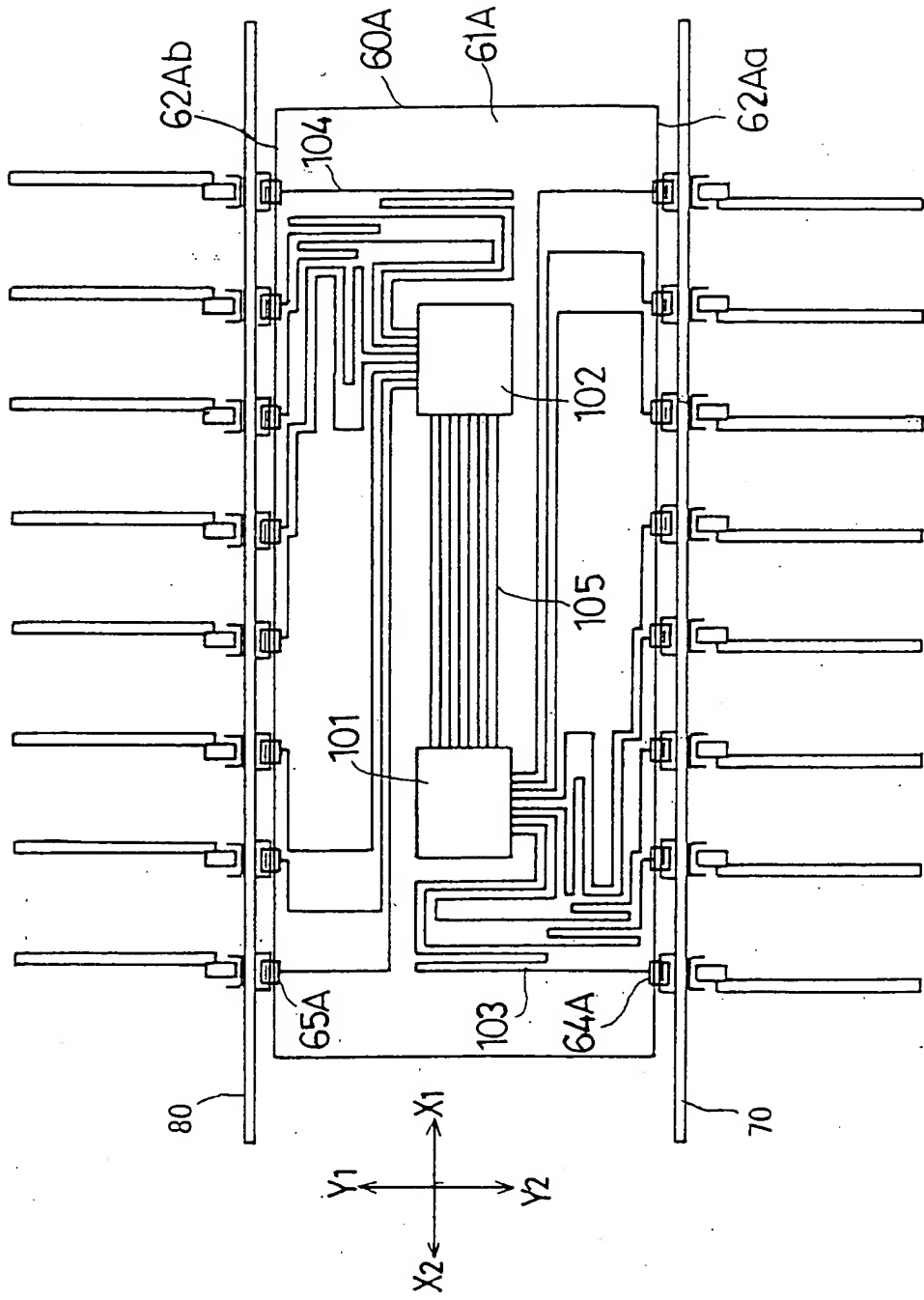


FIG. 7

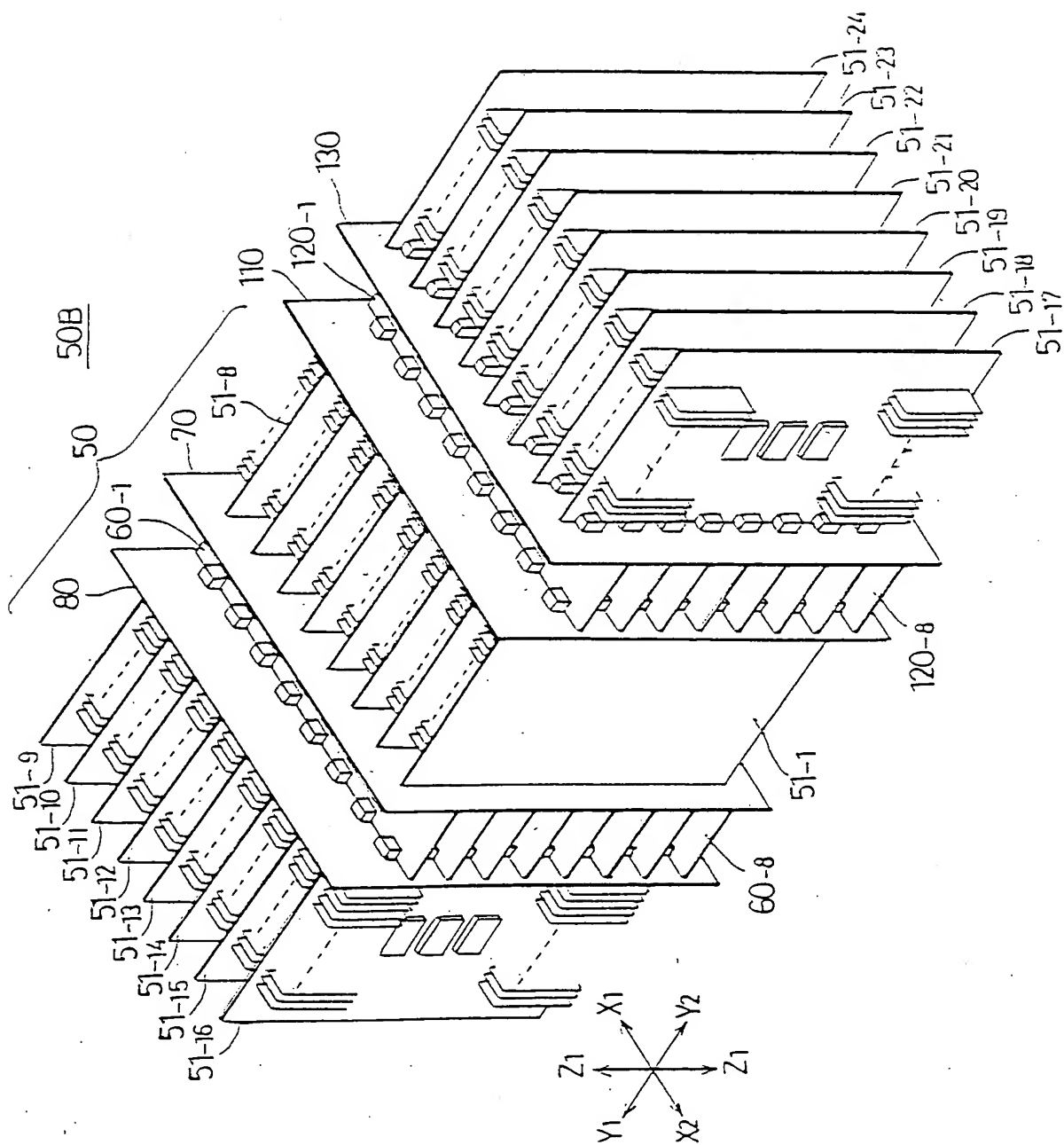


FIG. 8

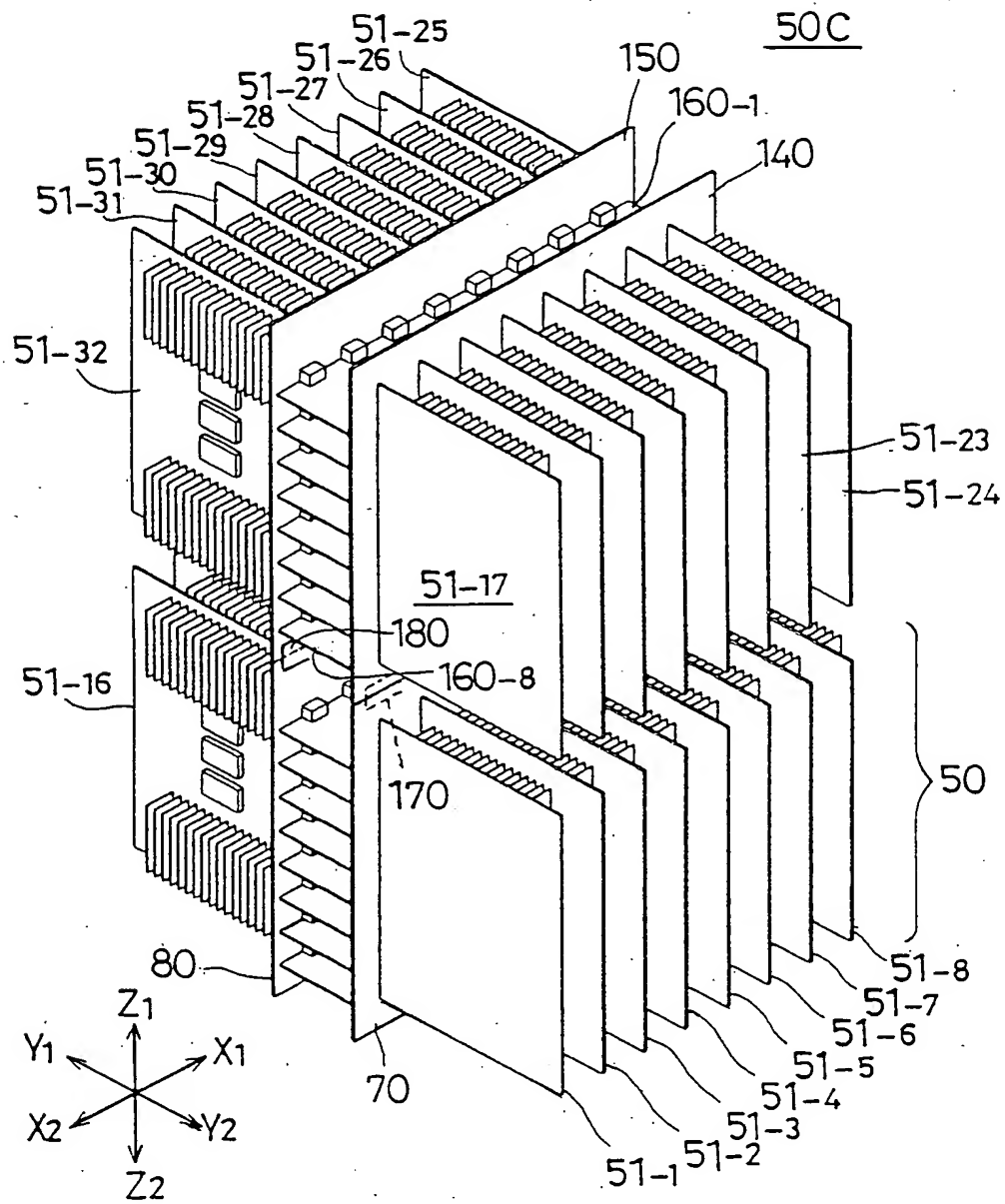




FIG. 9

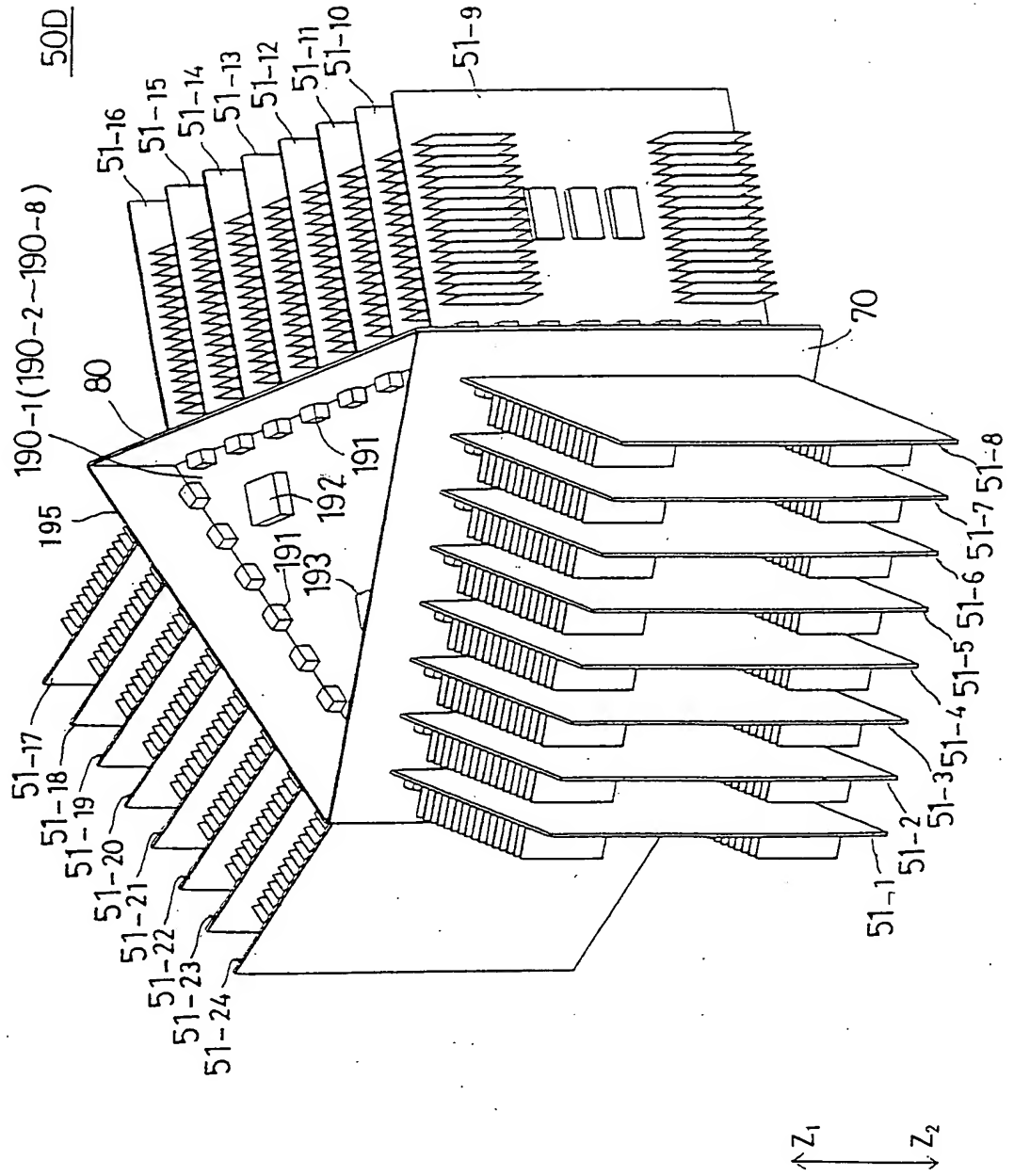


FIG. 10

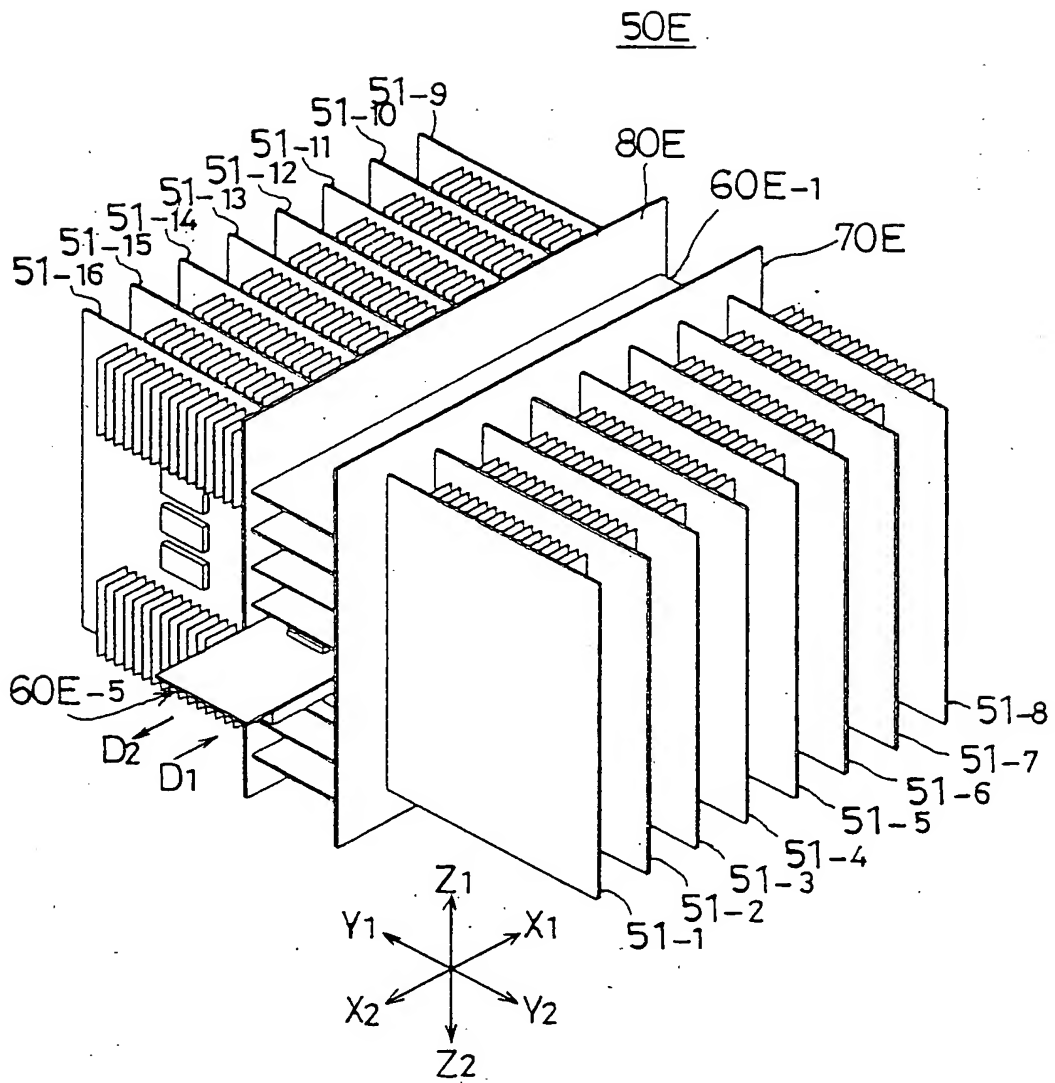


Figure 1 is a schematic diagram of a semiconductor device, showing a plan view and a cross-sectional view.

The plan view (top) shows a substrate 51-1b with a central region 53 and two side regions 54. A series of rectangular elements 200 and 202 are arranged in a row, connected by lines 201 and 203. A coordinate system (Y1, Y2, Z1, Z2) is shown at the bottom left.

The cross-sectional view (bottom) shows the vertical structure of the device. It includes a substrate 51-1, a layer 60E-5, a layer 60E-8, a layer 70E, a layer 73E, a layer 80E, and a layer 83E. A contact region 61 is shown, with sub-regions 61a and 61b. A layer 200 is also indicated.

FIG. 12

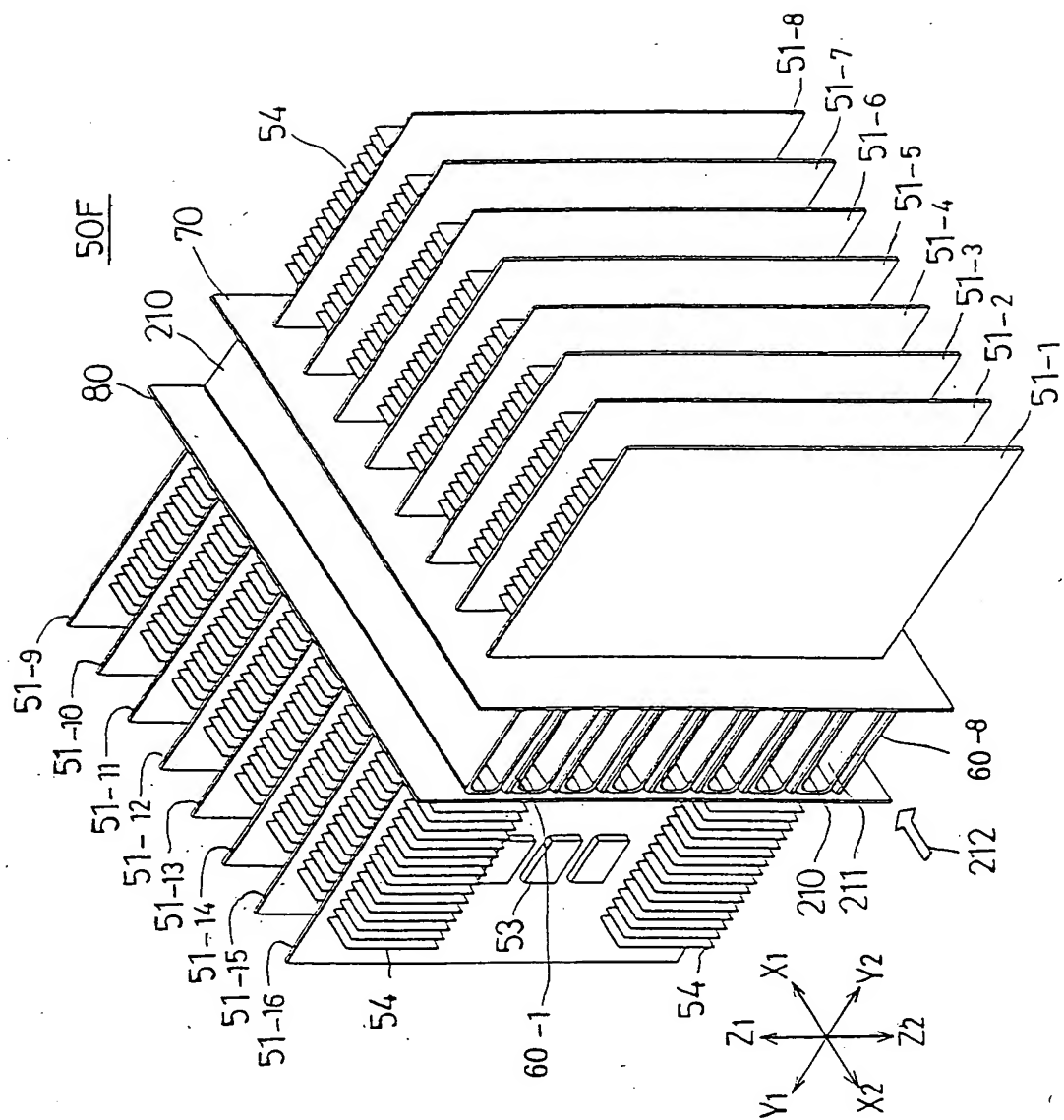


FIG. 13

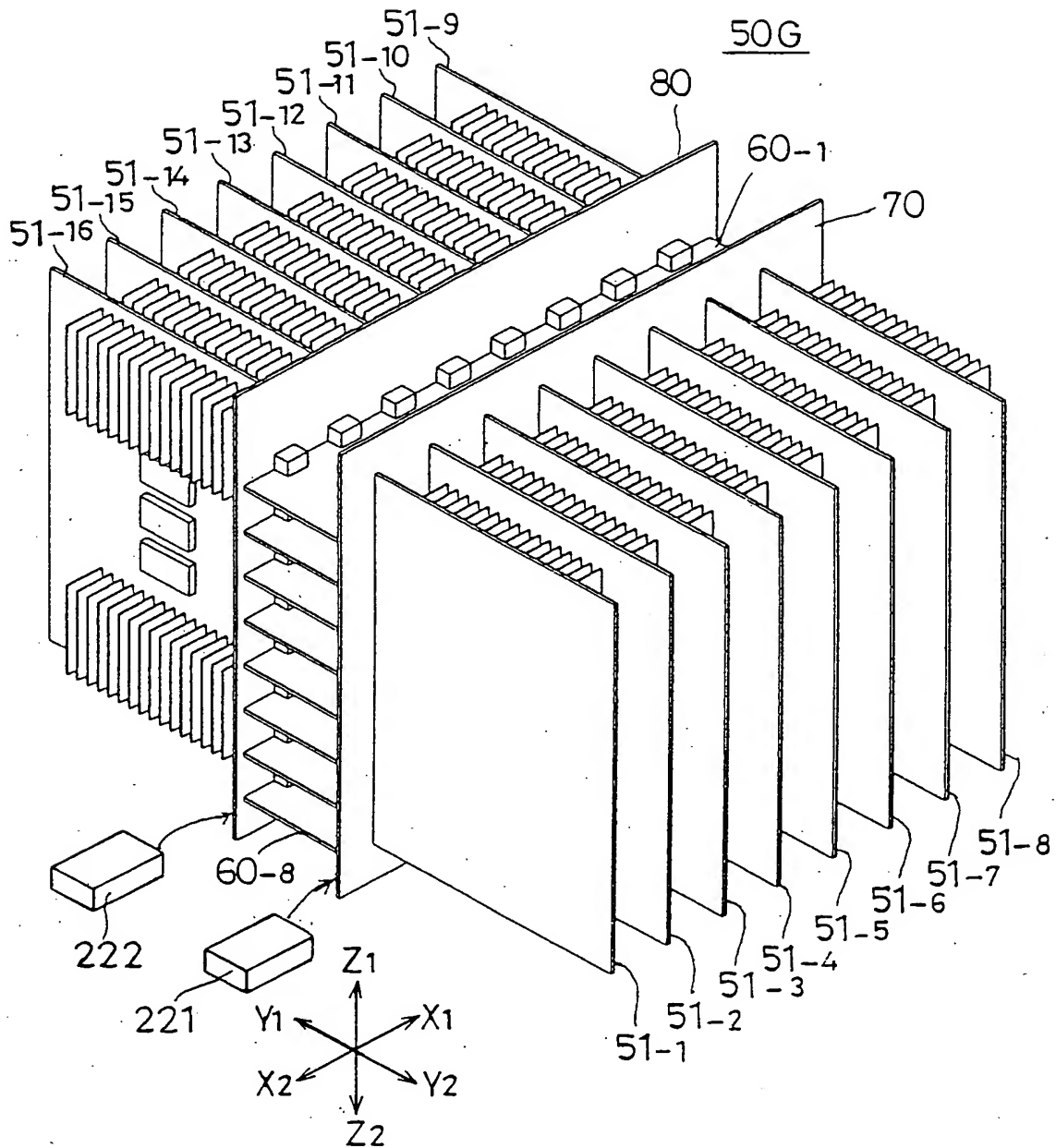


FIG. 14

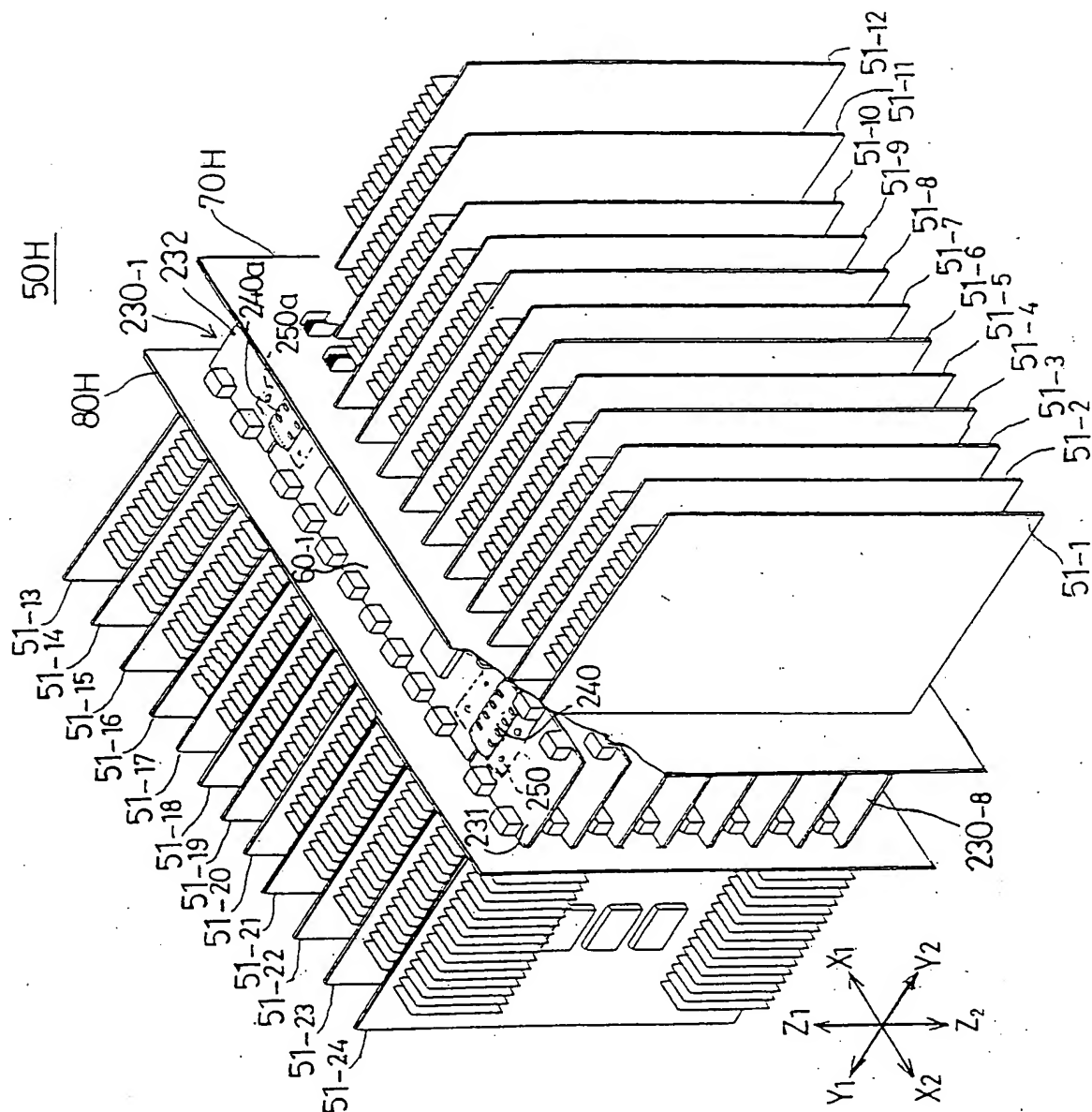


FIG. 15

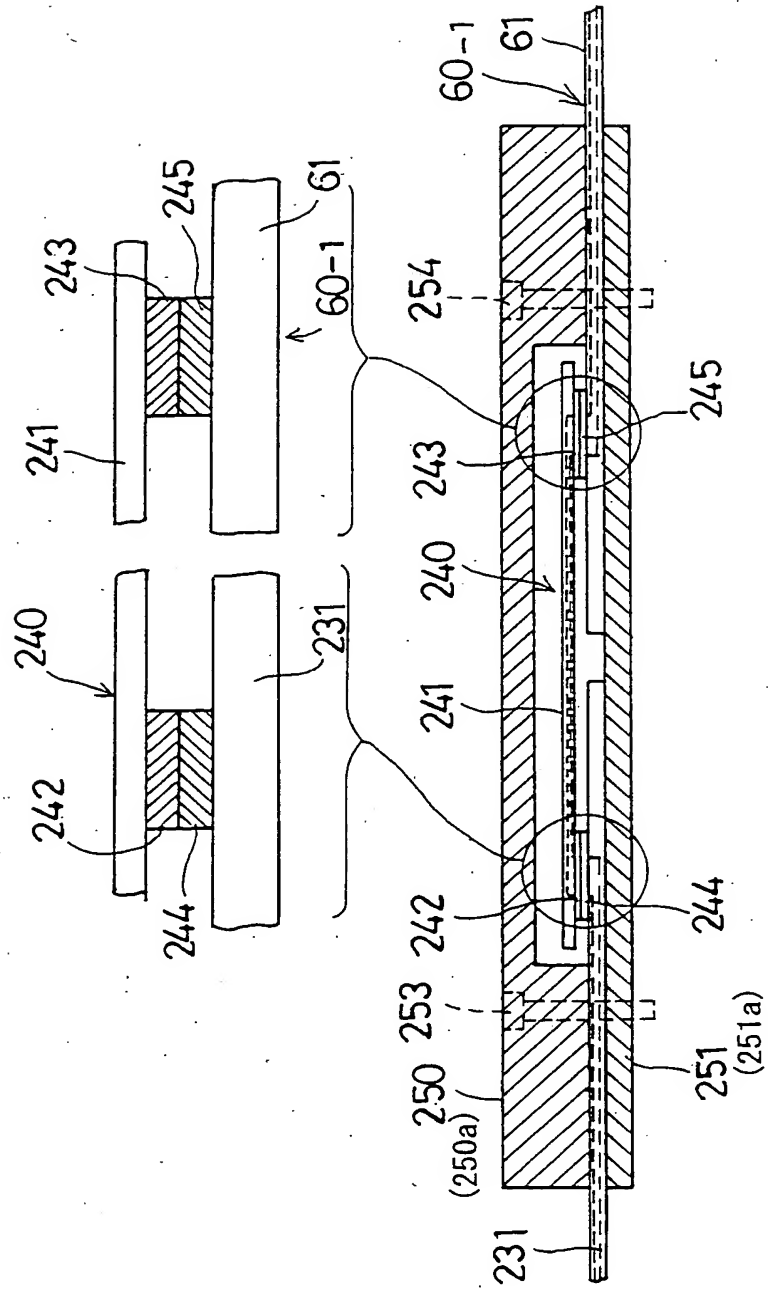


FIG. 16

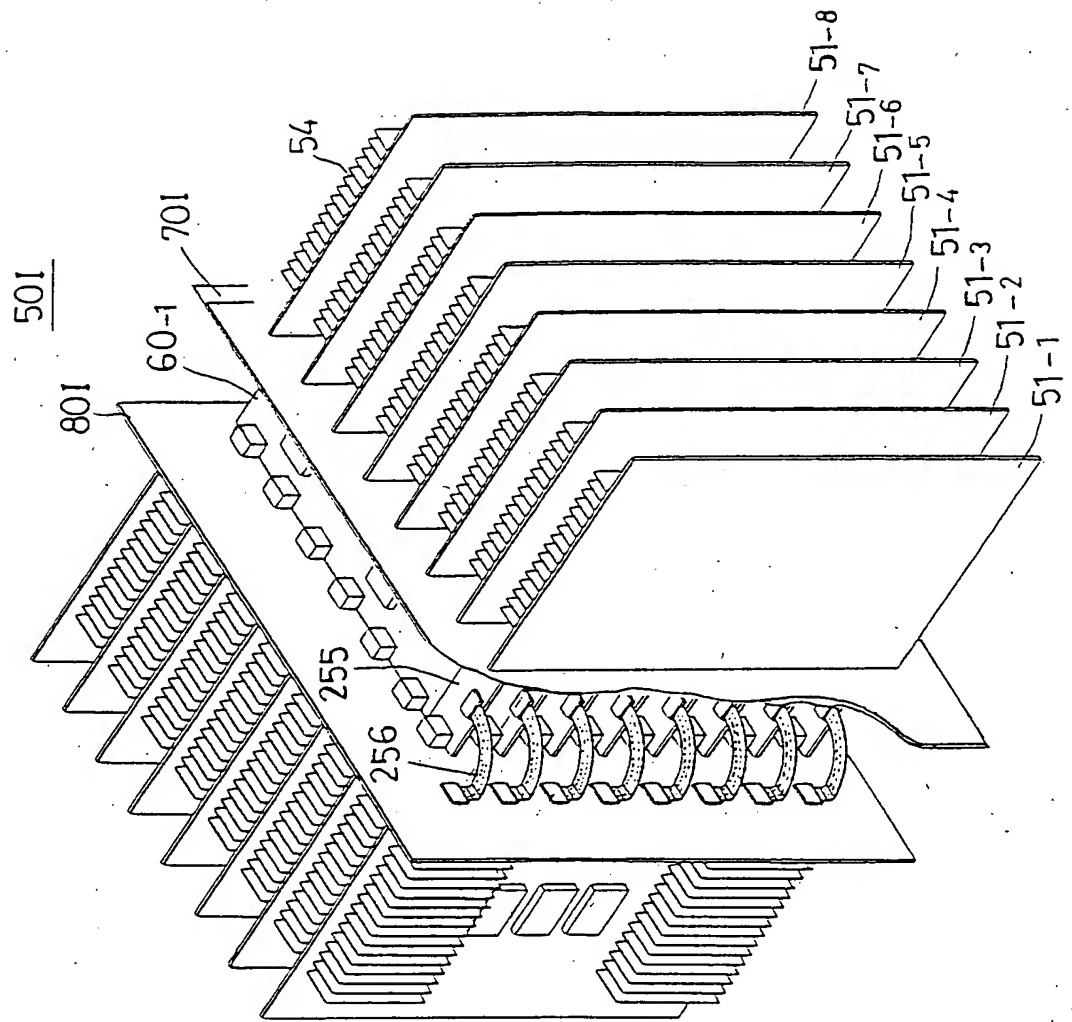




FIG. 17

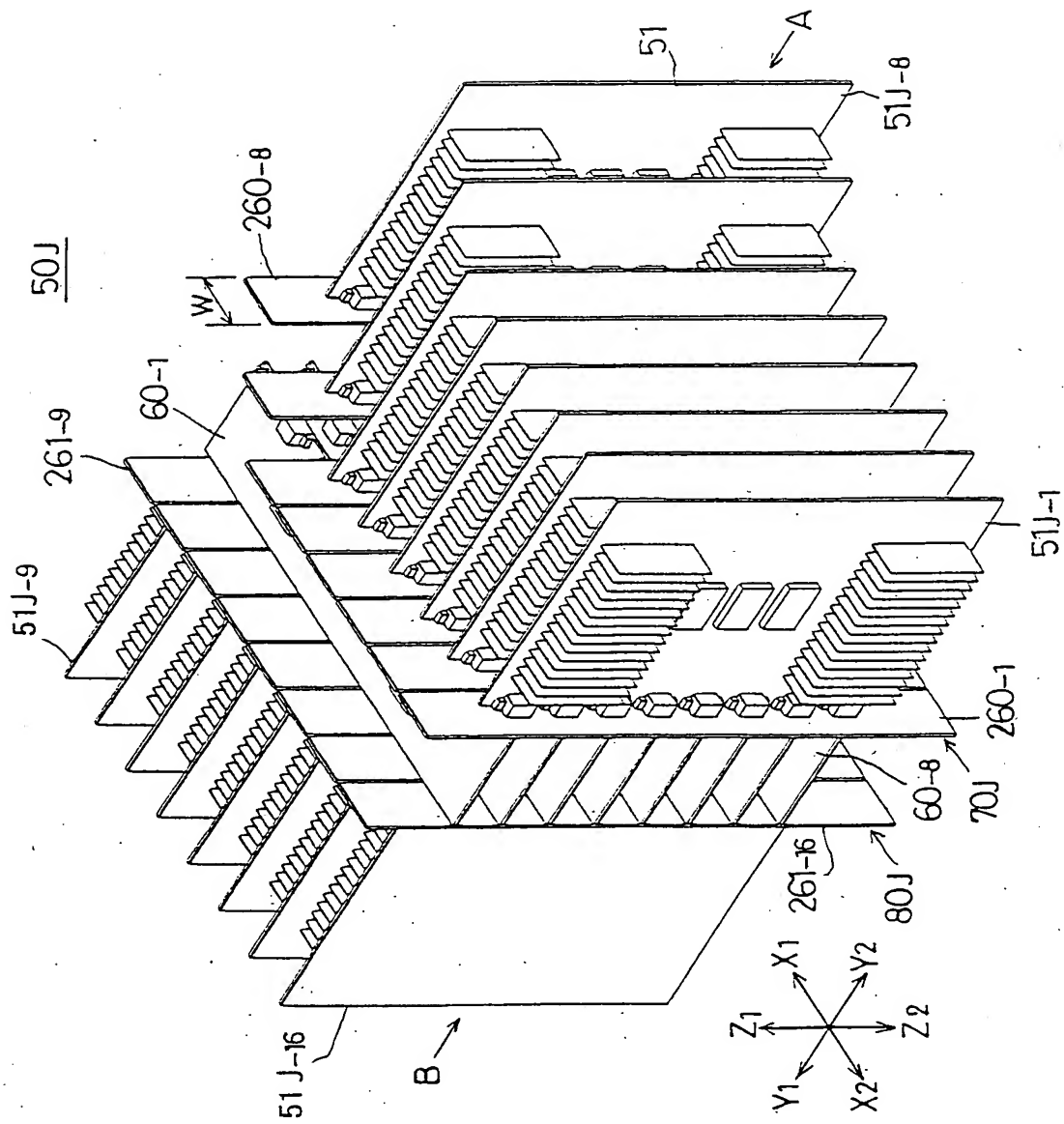


FIG. 18

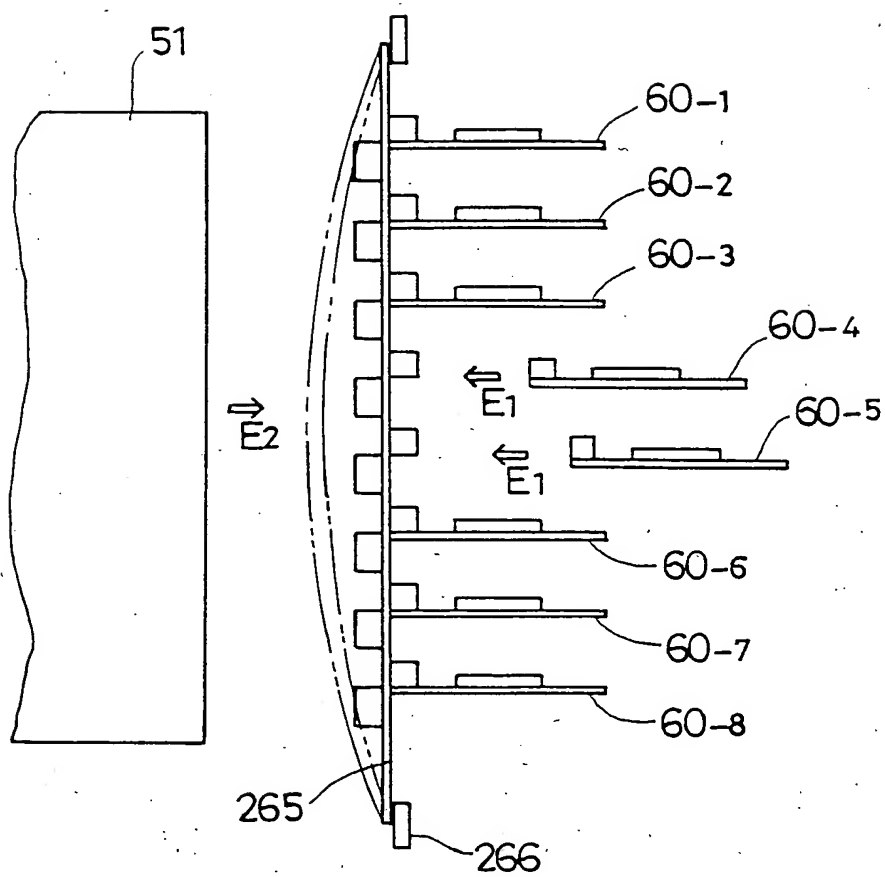


FIG. 19

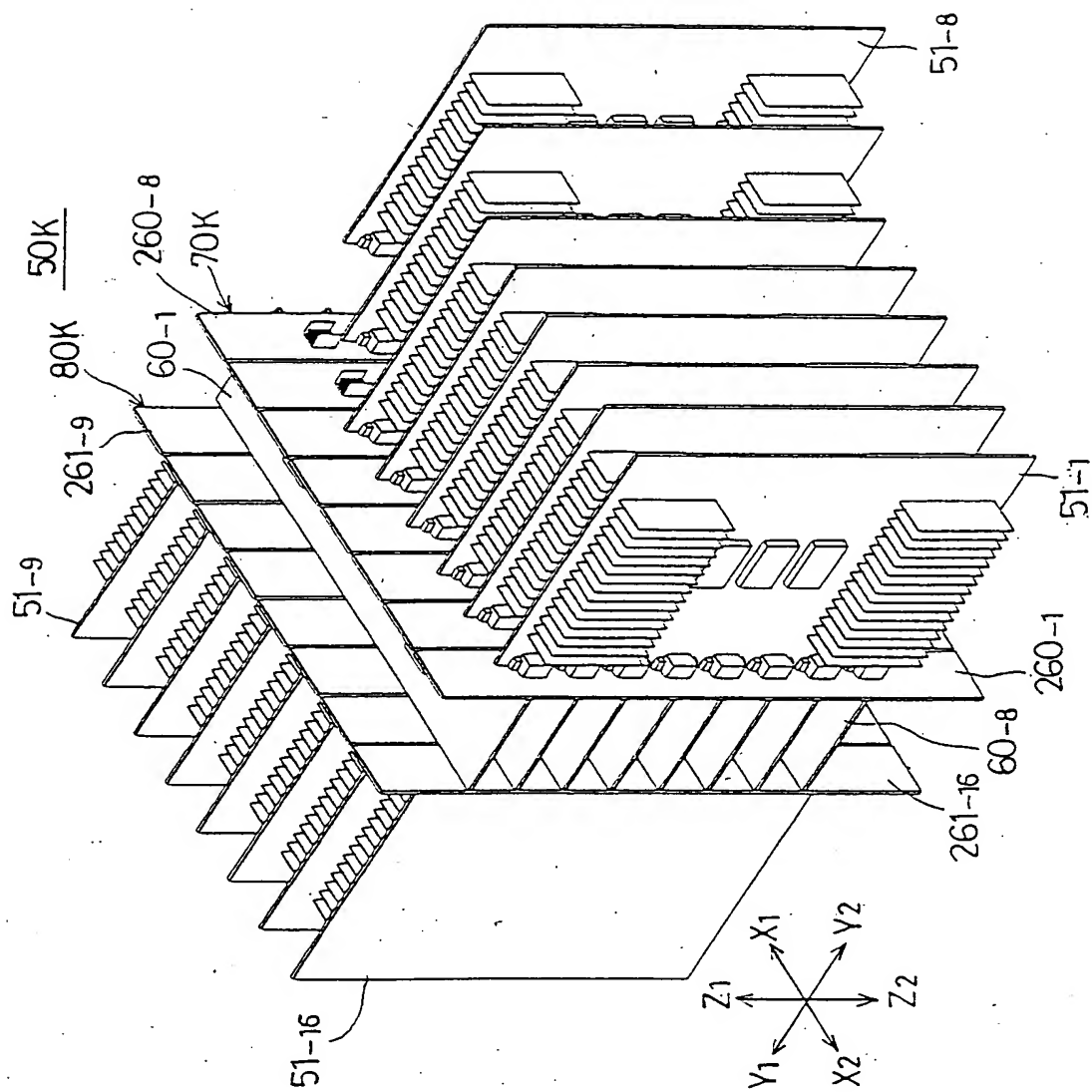


FIG. 20

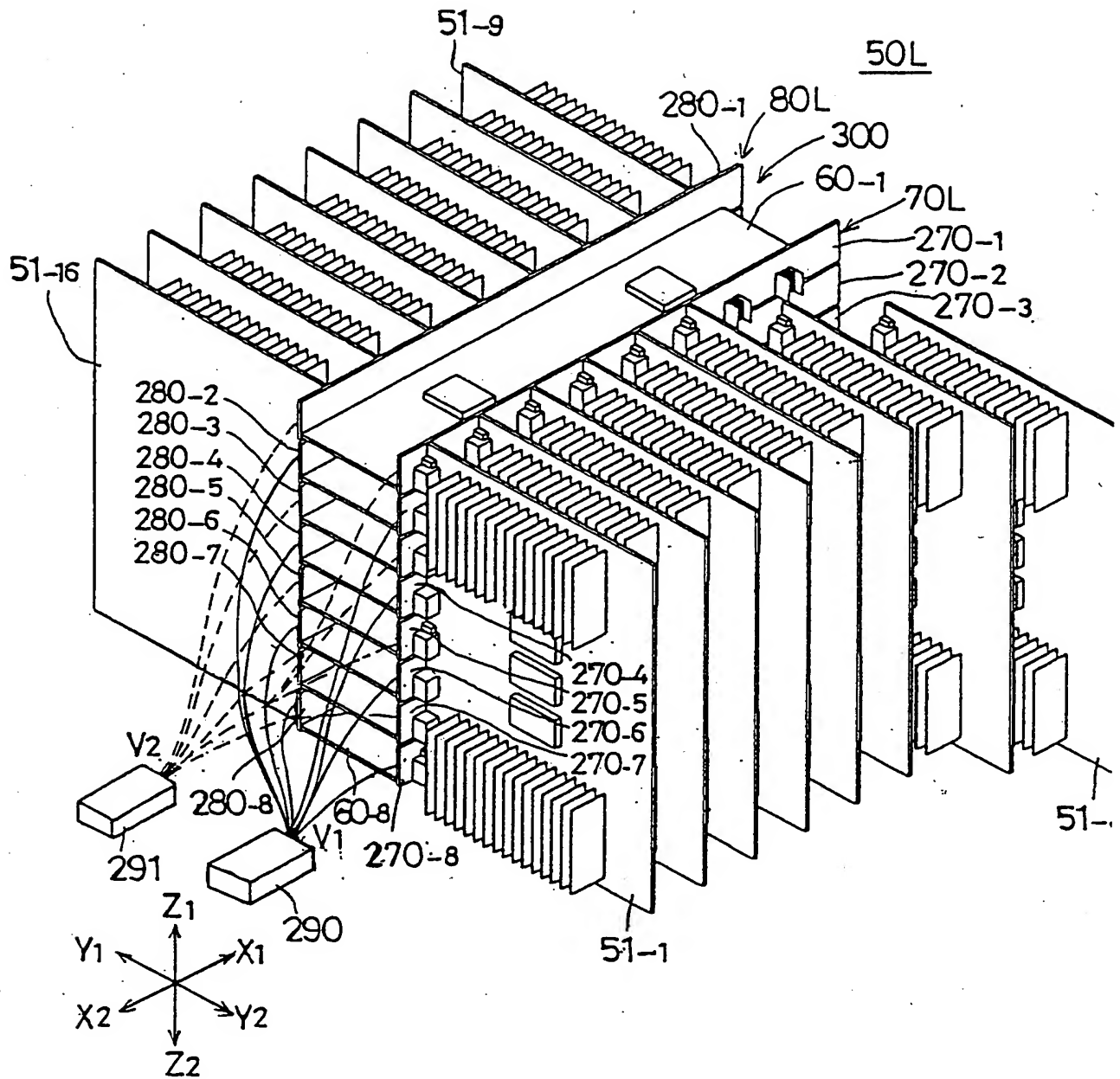


FIG. 21

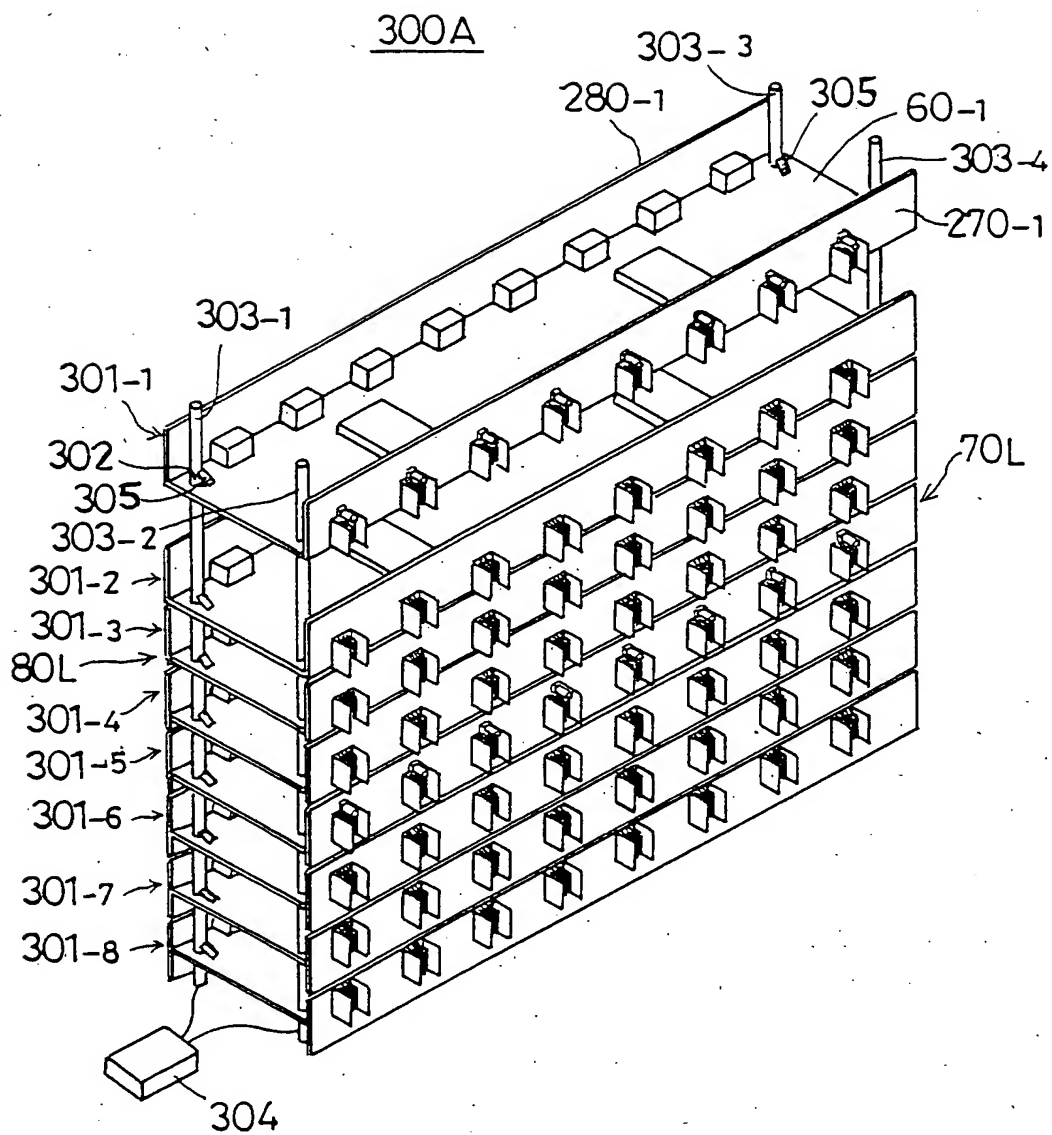


FIG. 22

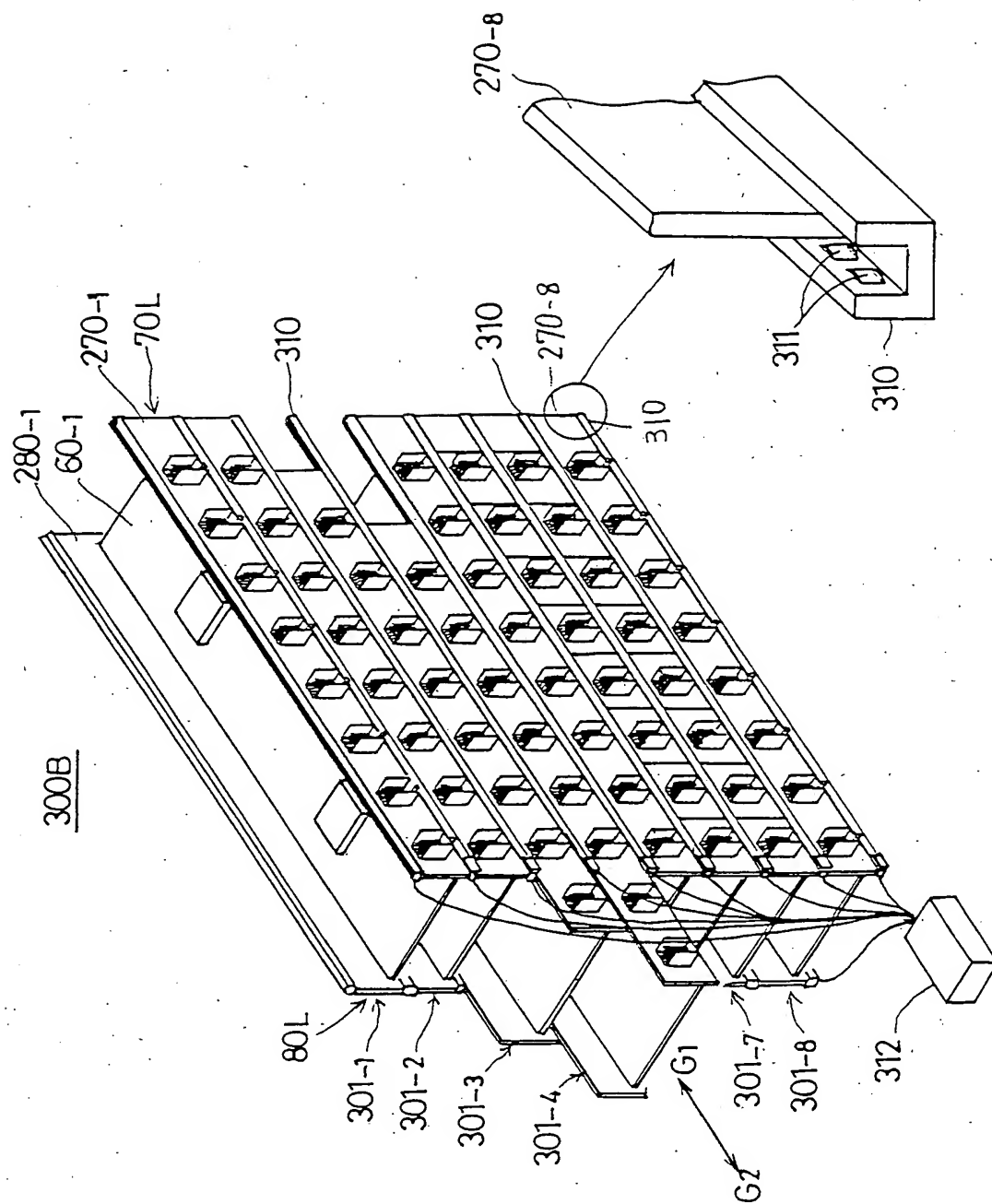


FIG. 23

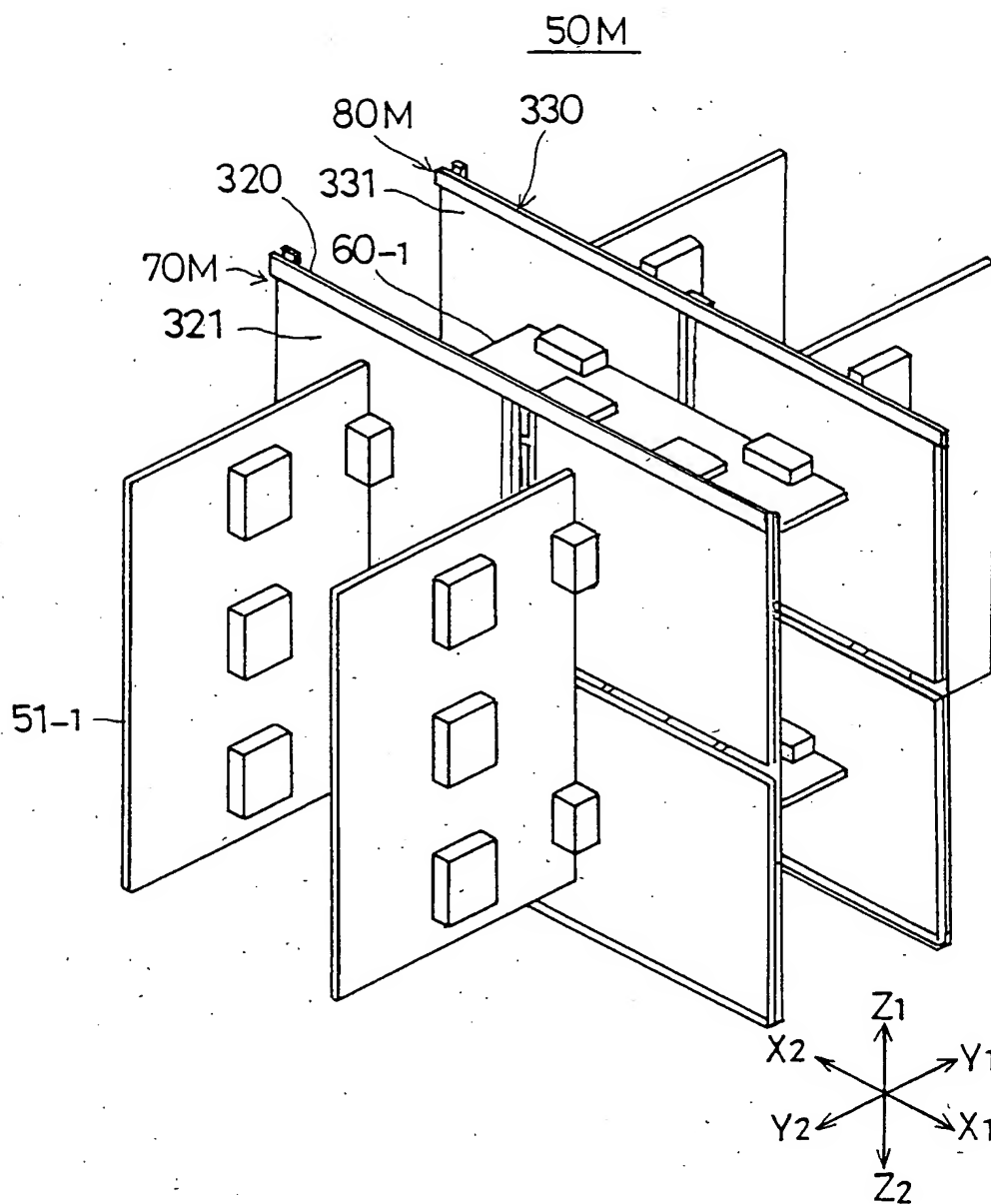


FIG. 24

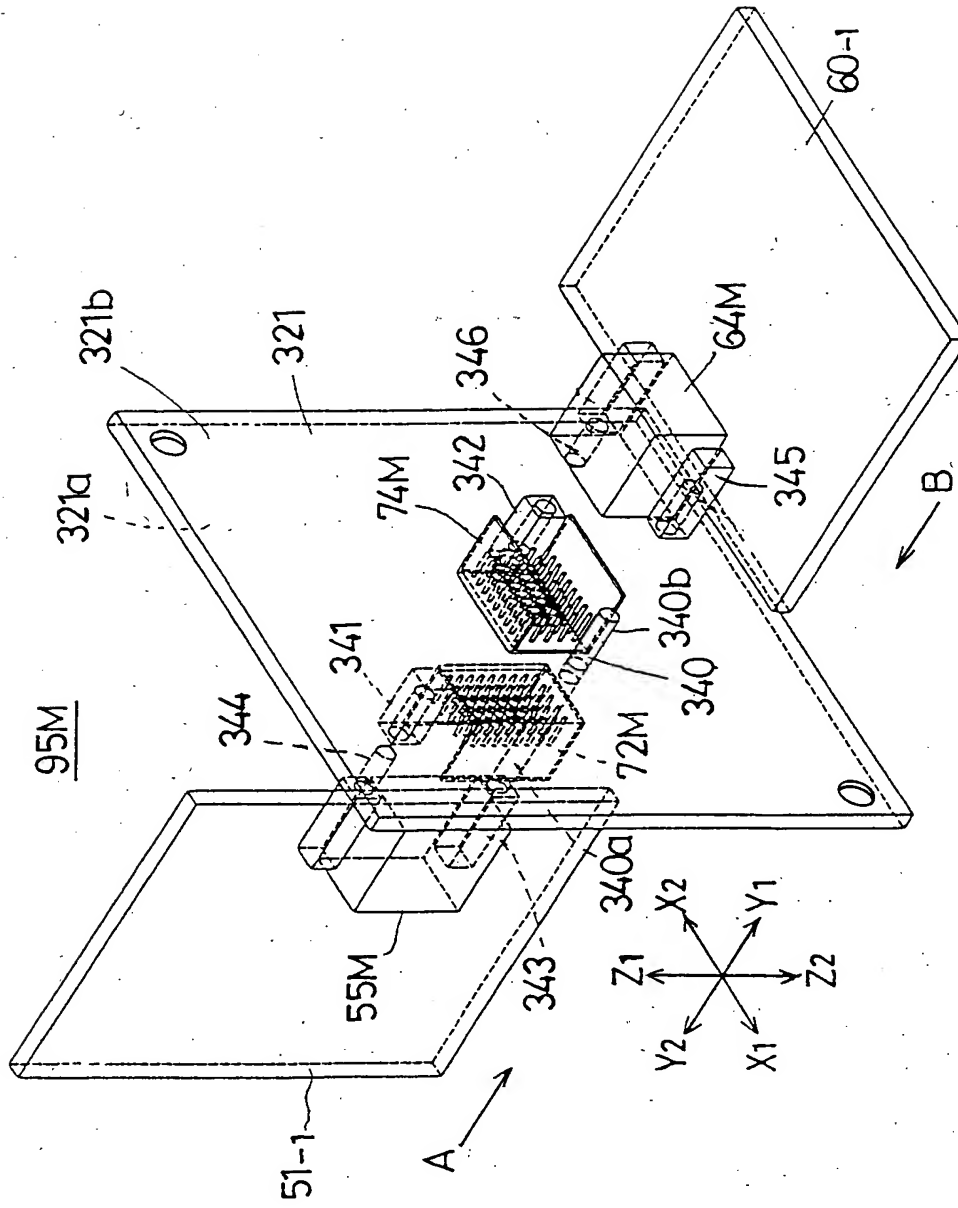






FIG. 26

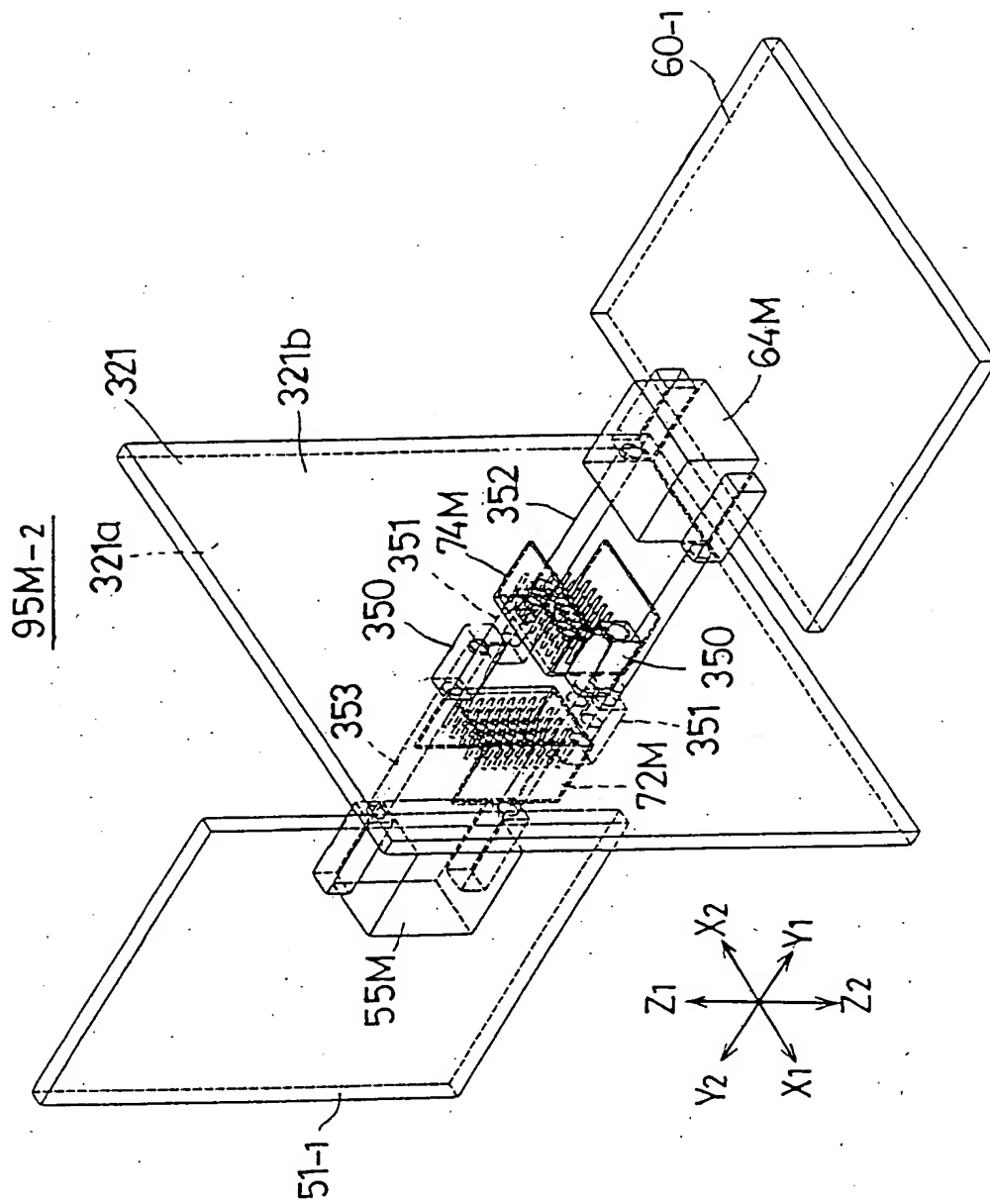


FIG. 27

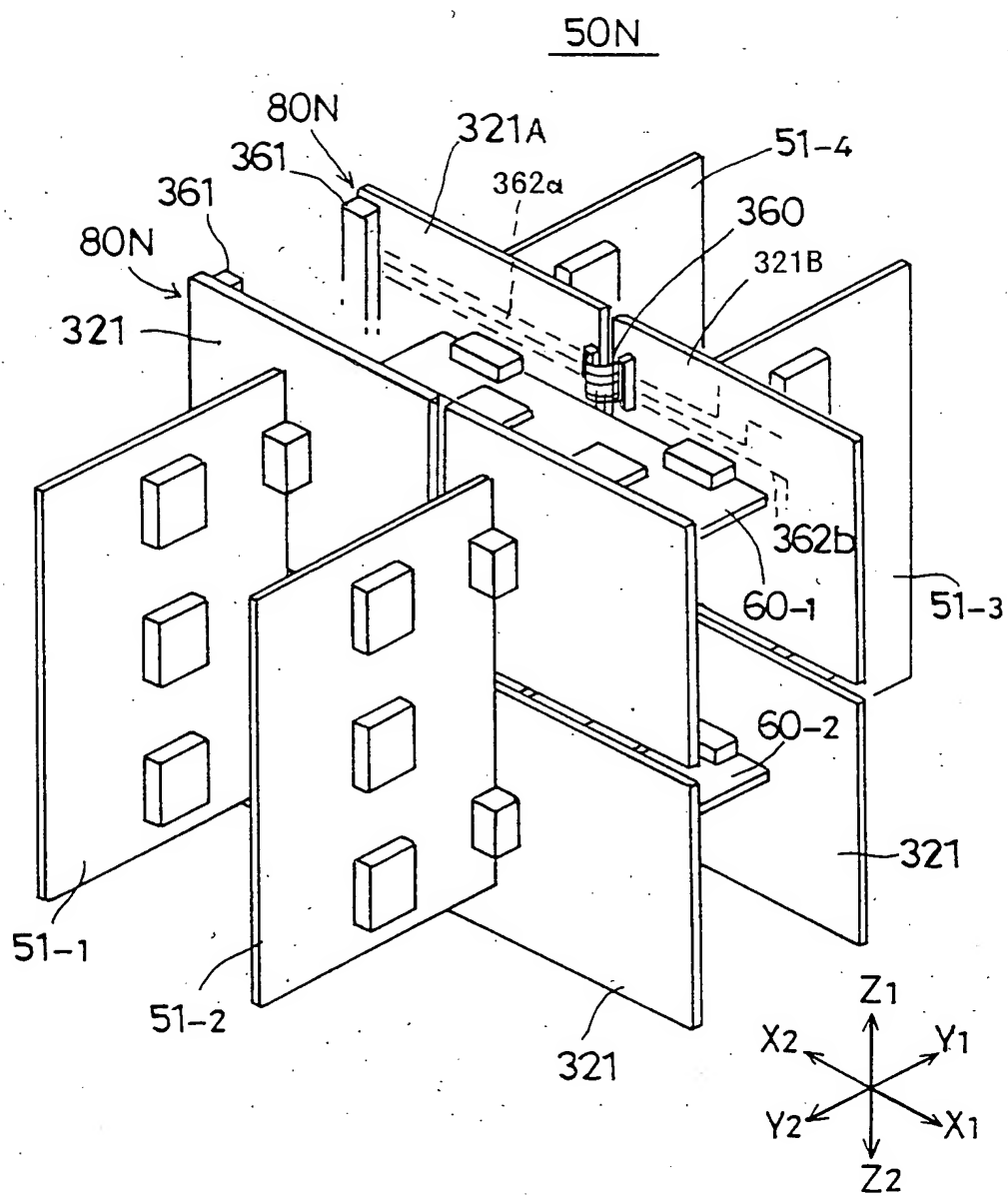


FIG. 28

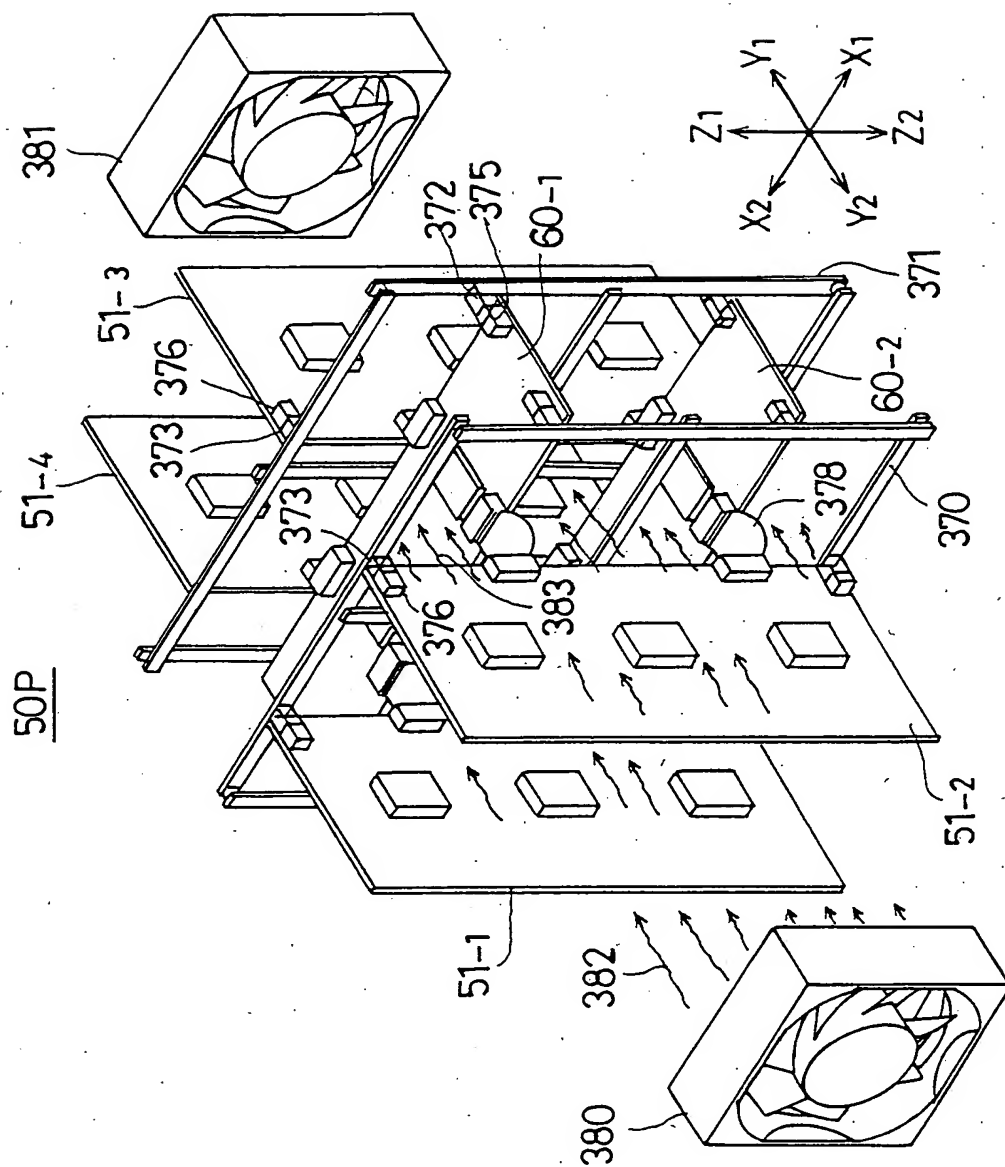


FIG. 29

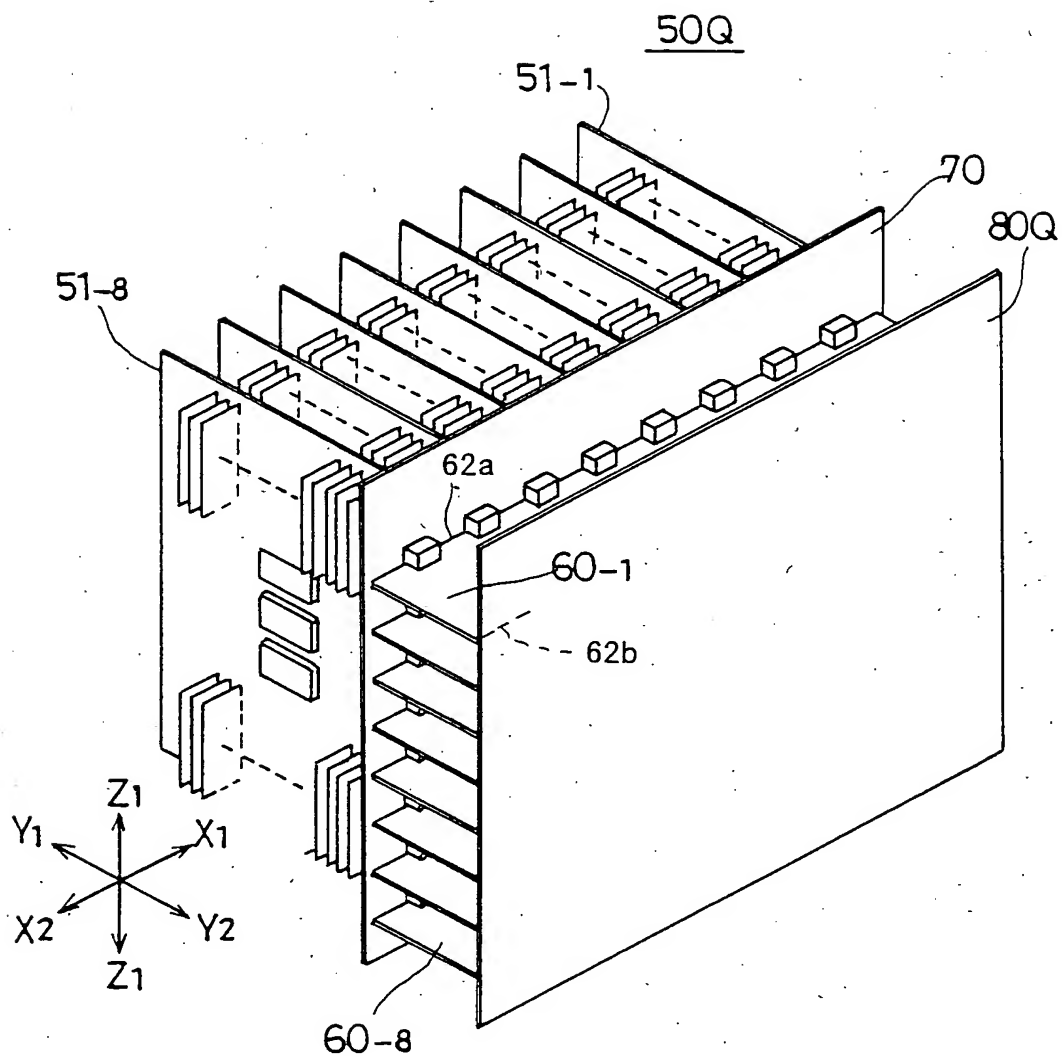


FIG. 30

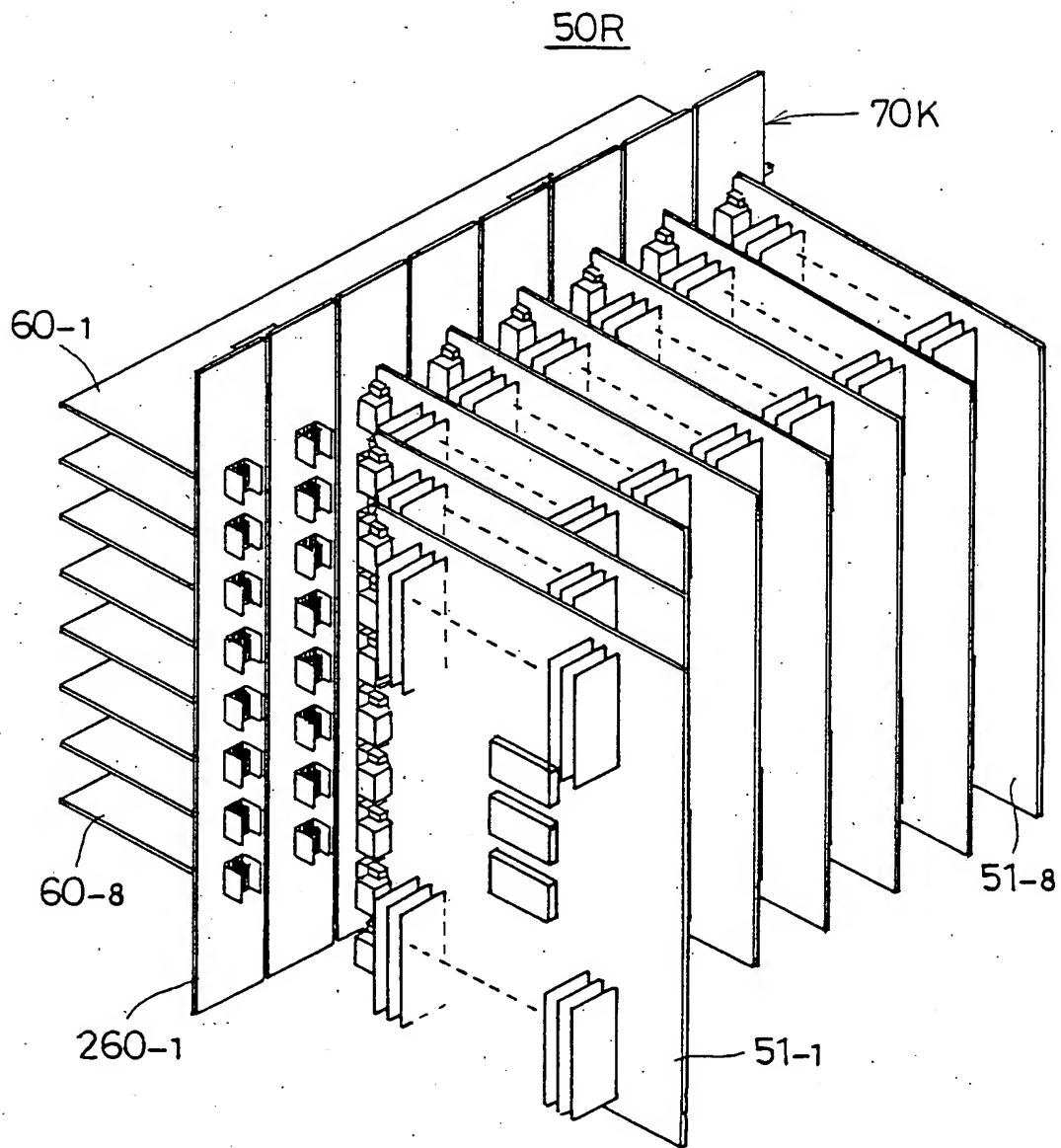


FIG. 31A

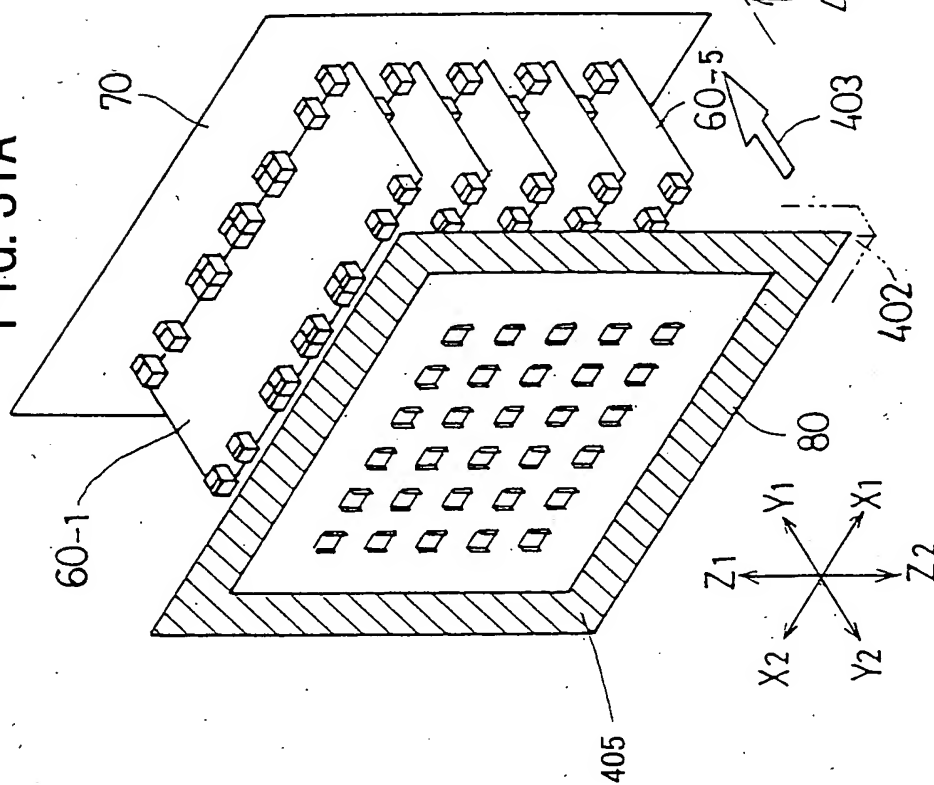


FIG. 31B

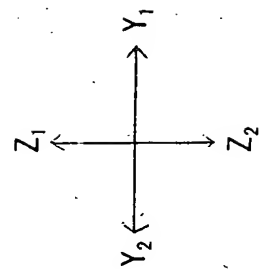
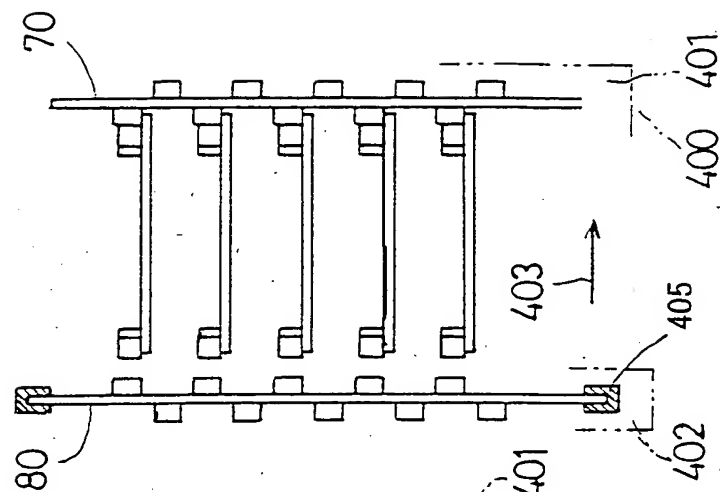


FIG. 32A

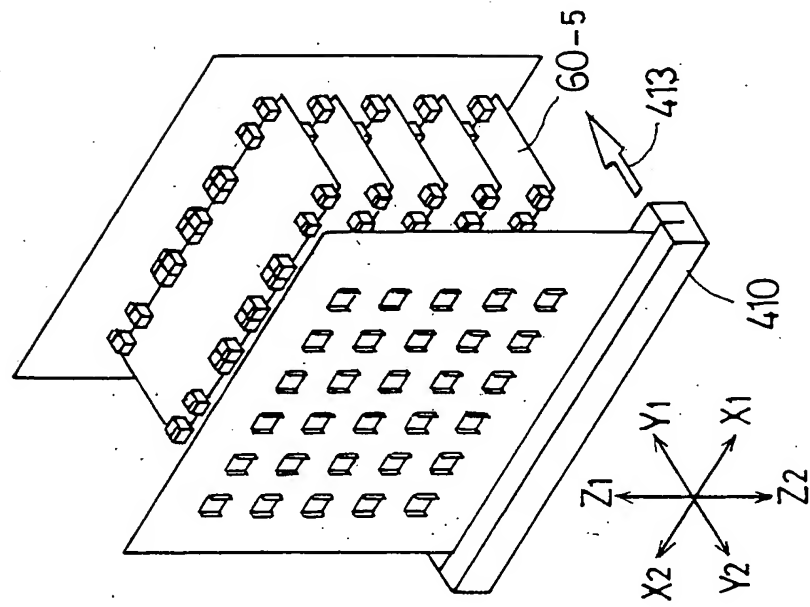


FIG. 32B

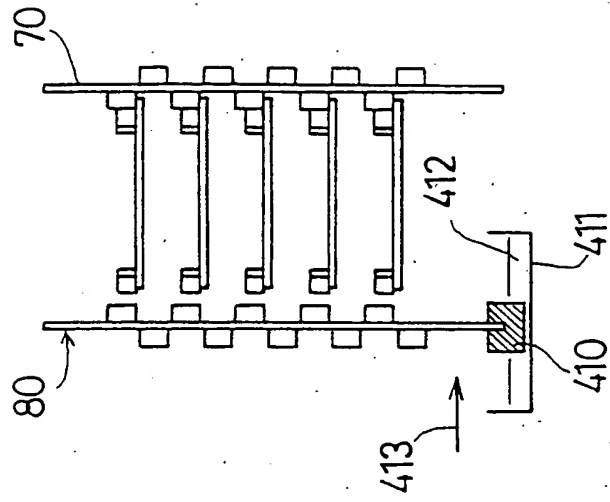




FIG. 33

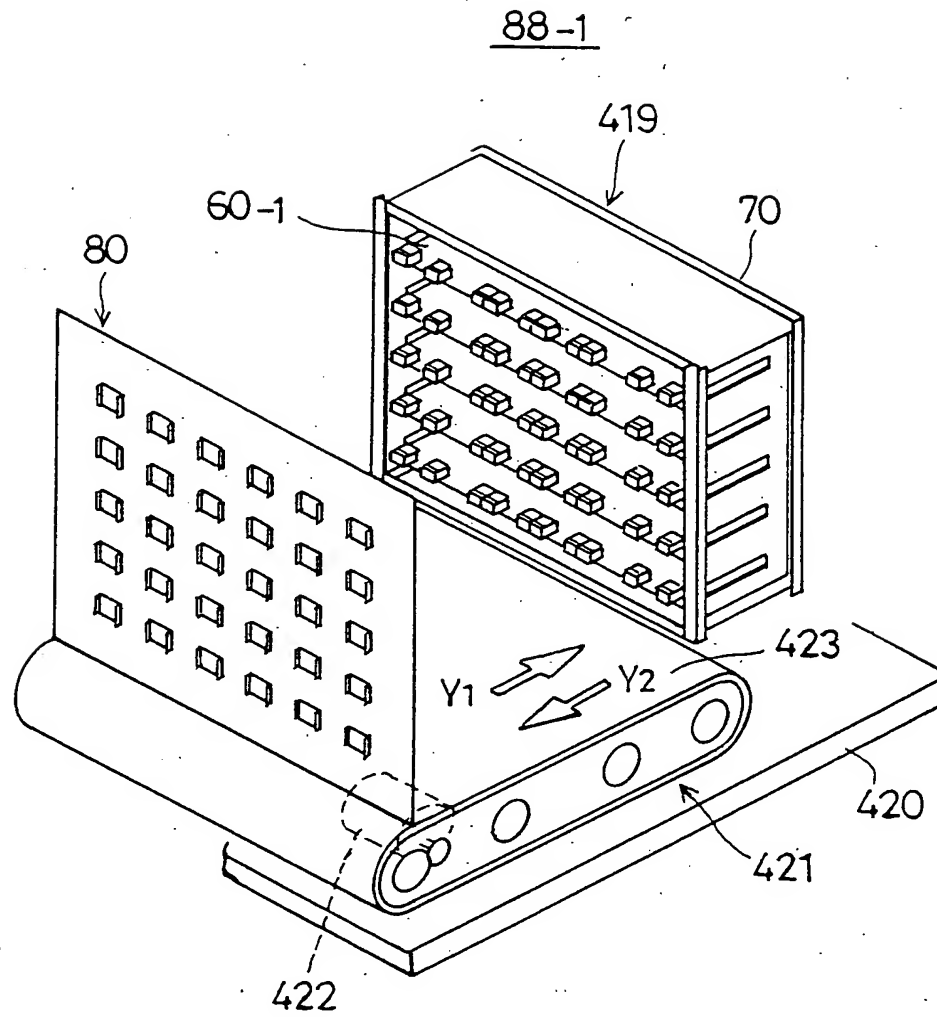


FIG. 34

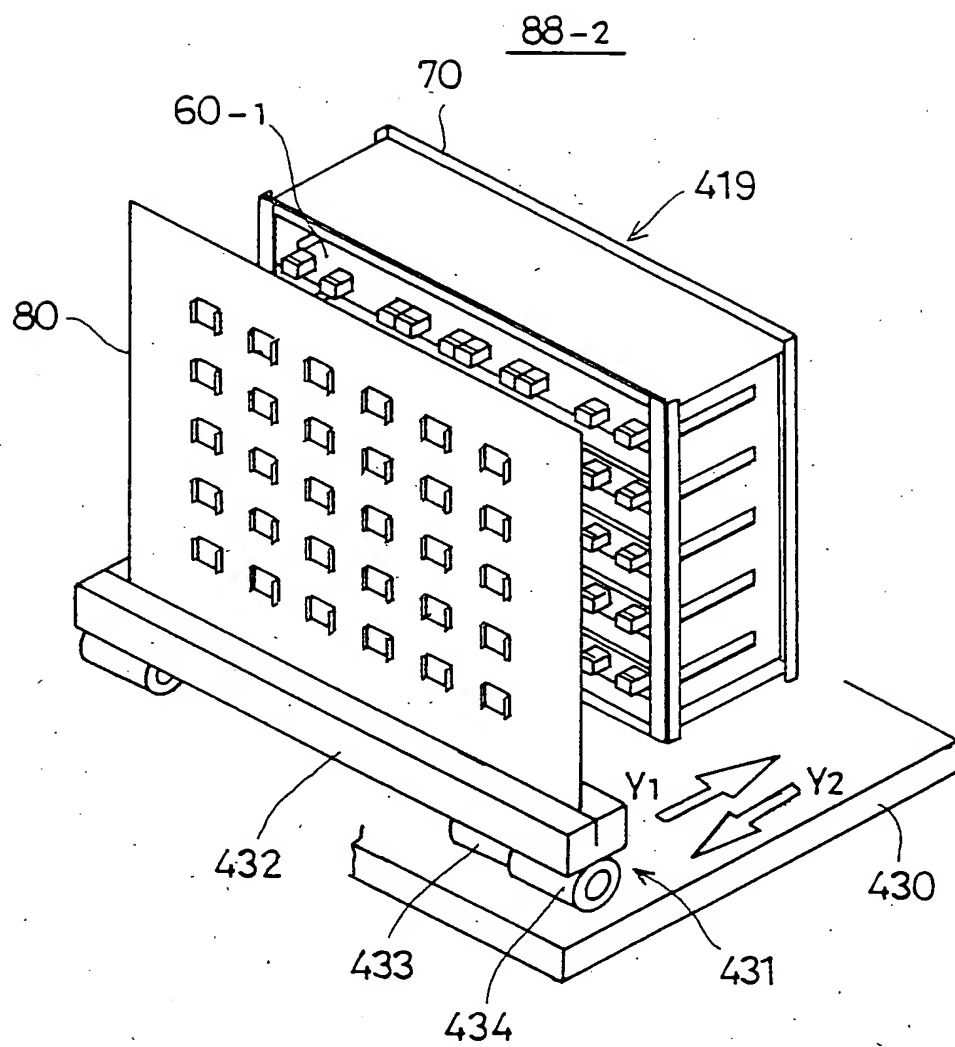


FIG. 35A

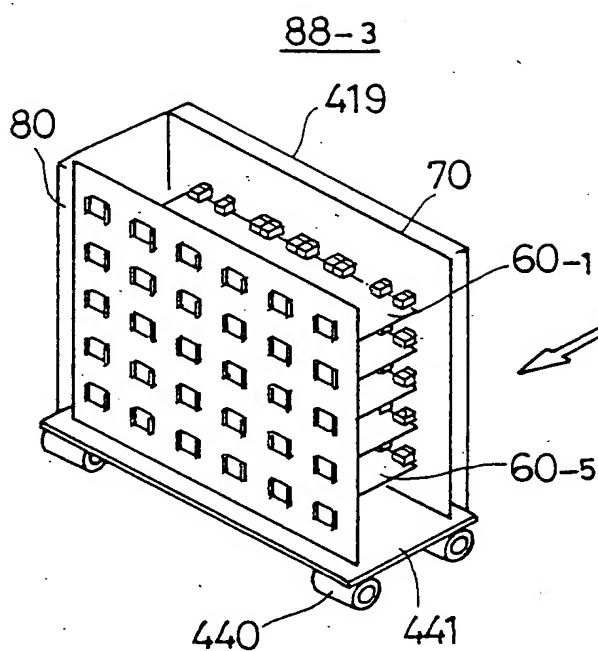


FIG. 35B

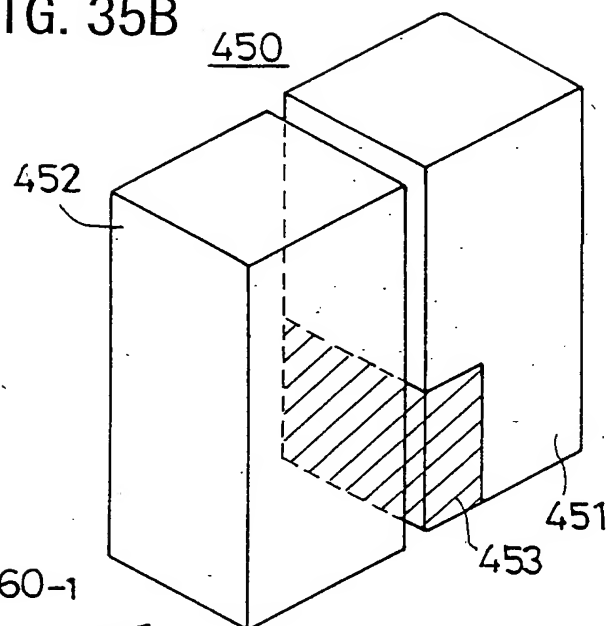


FIG. 35C

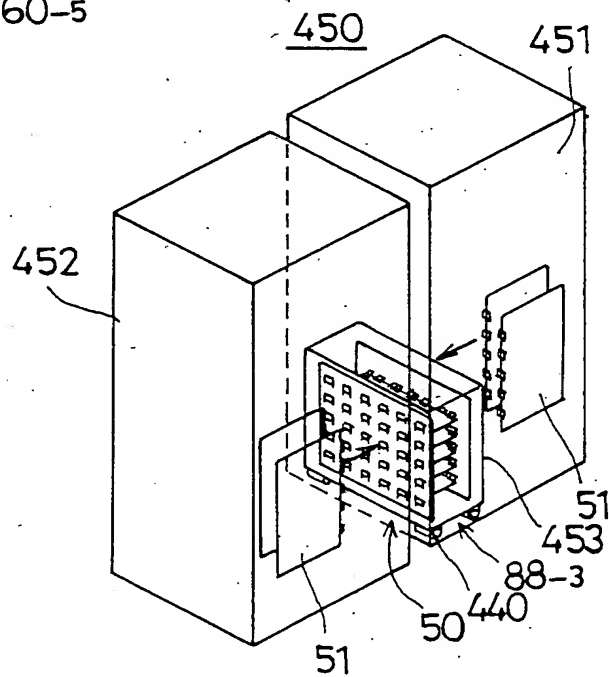


FIG. 36A

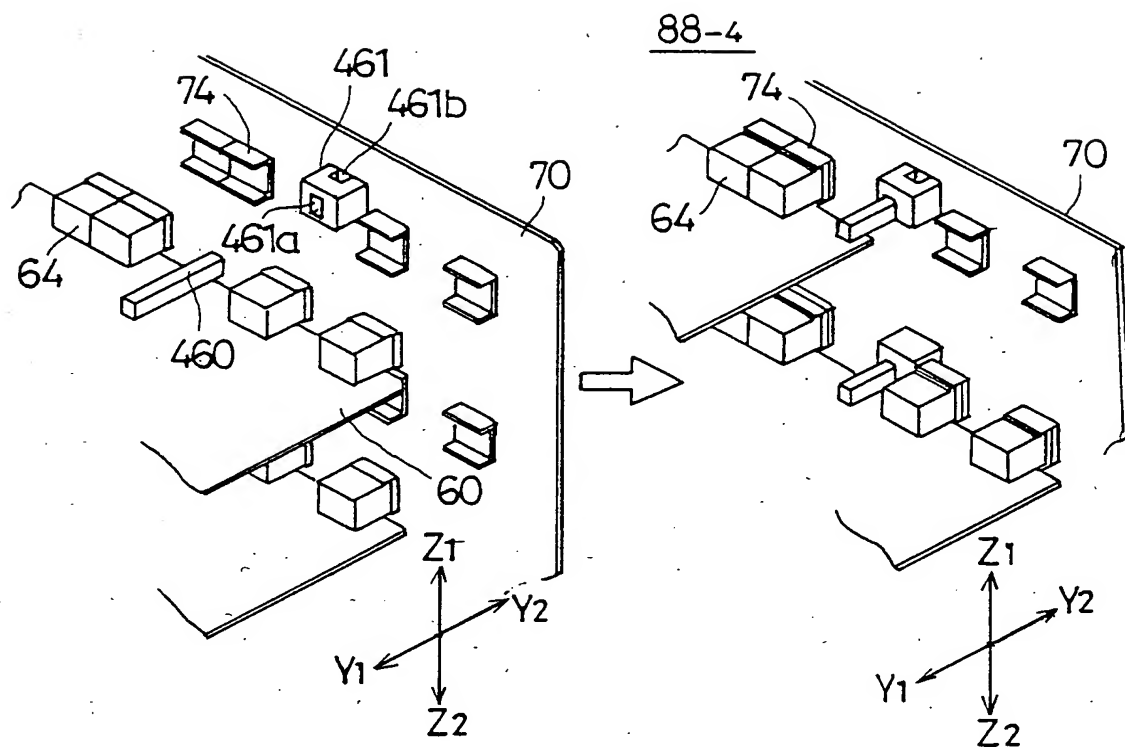


FIG. 36B

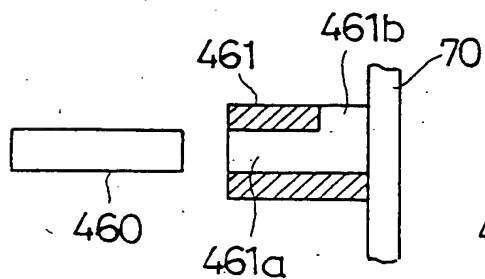


FIG. 36C

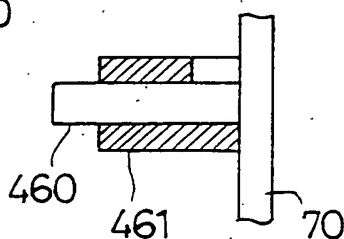


FIG. 36D

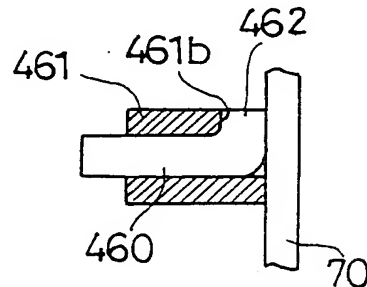


FIG. 37

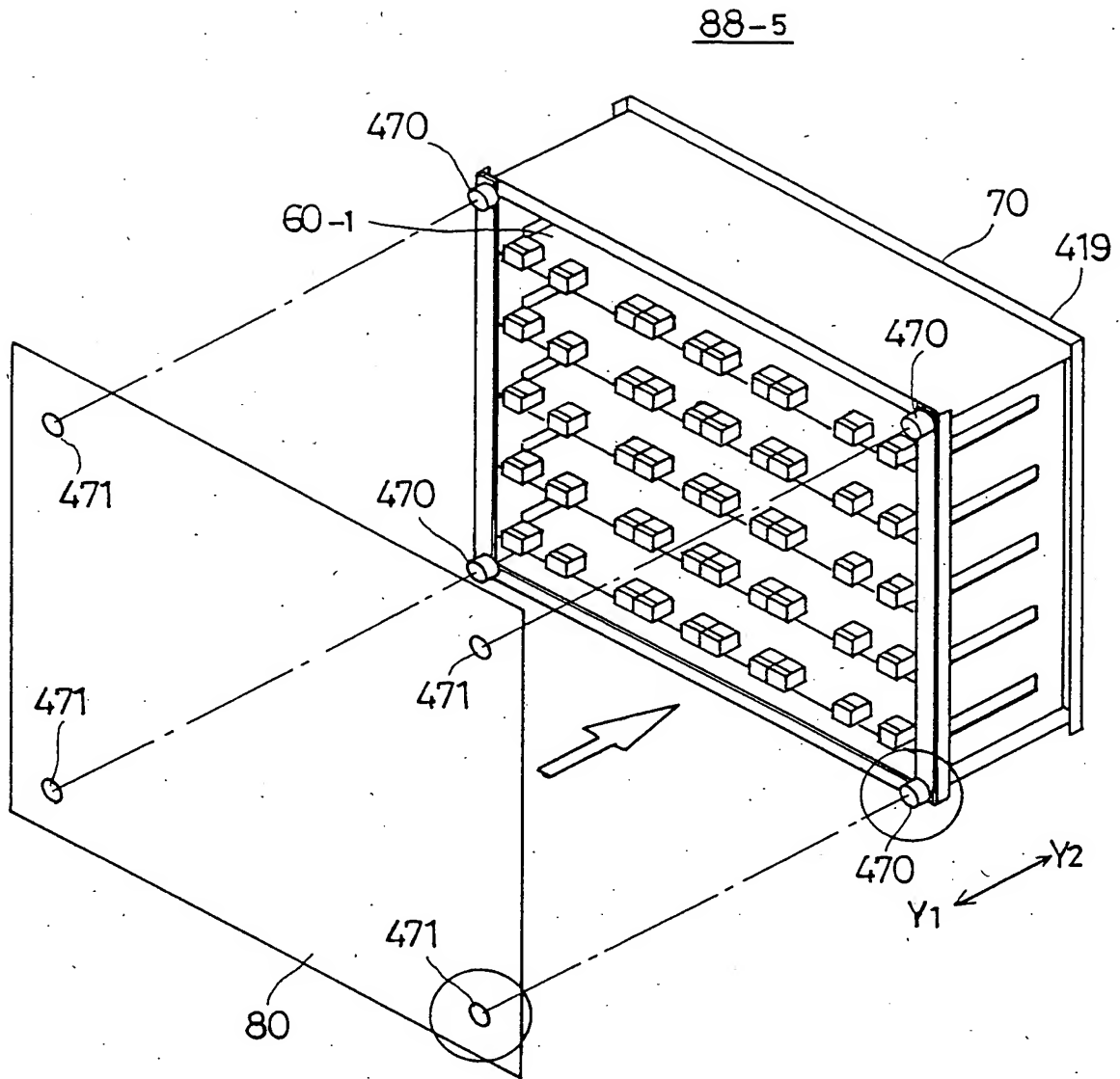


FIG. 38

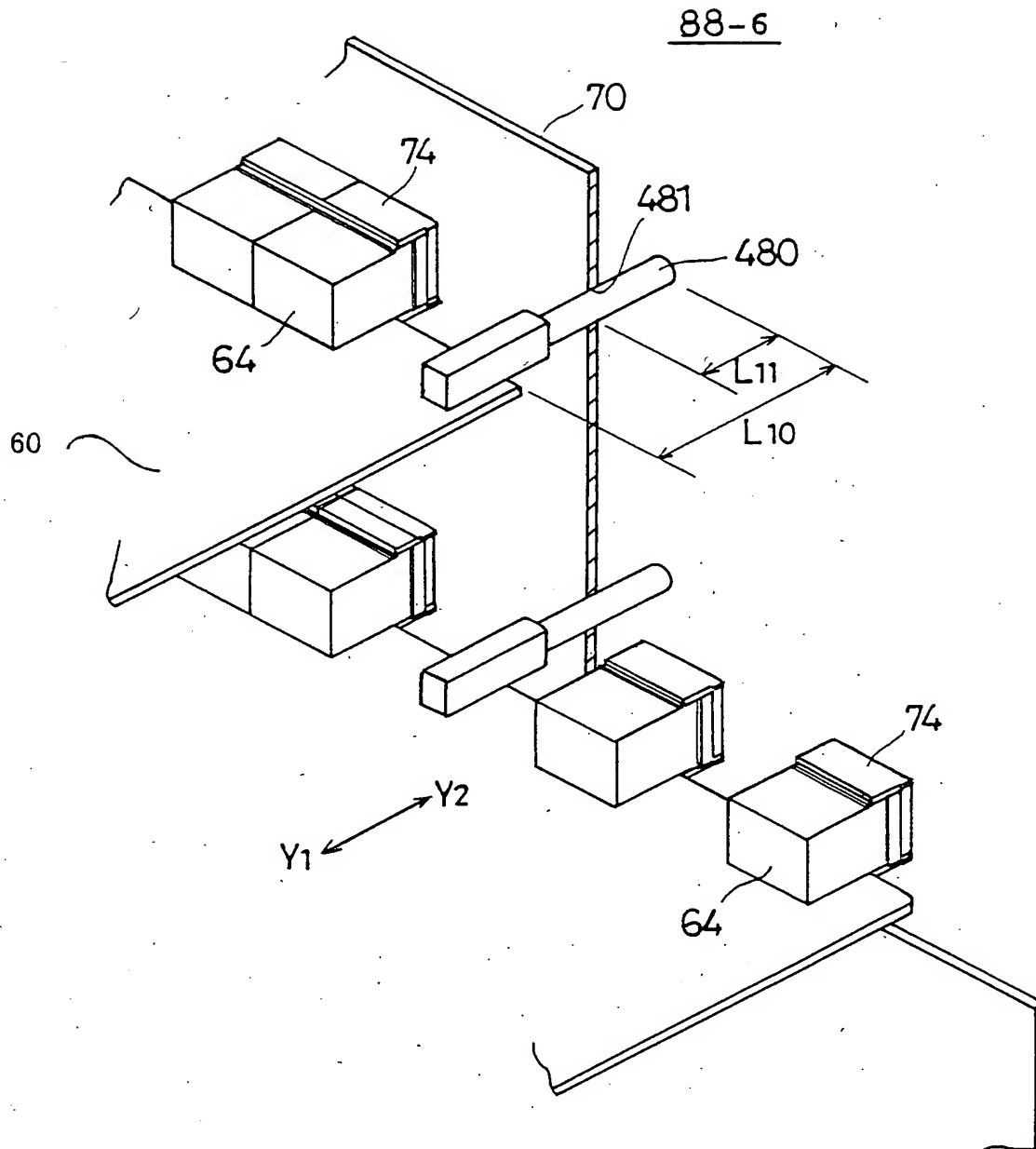


FIG. 39

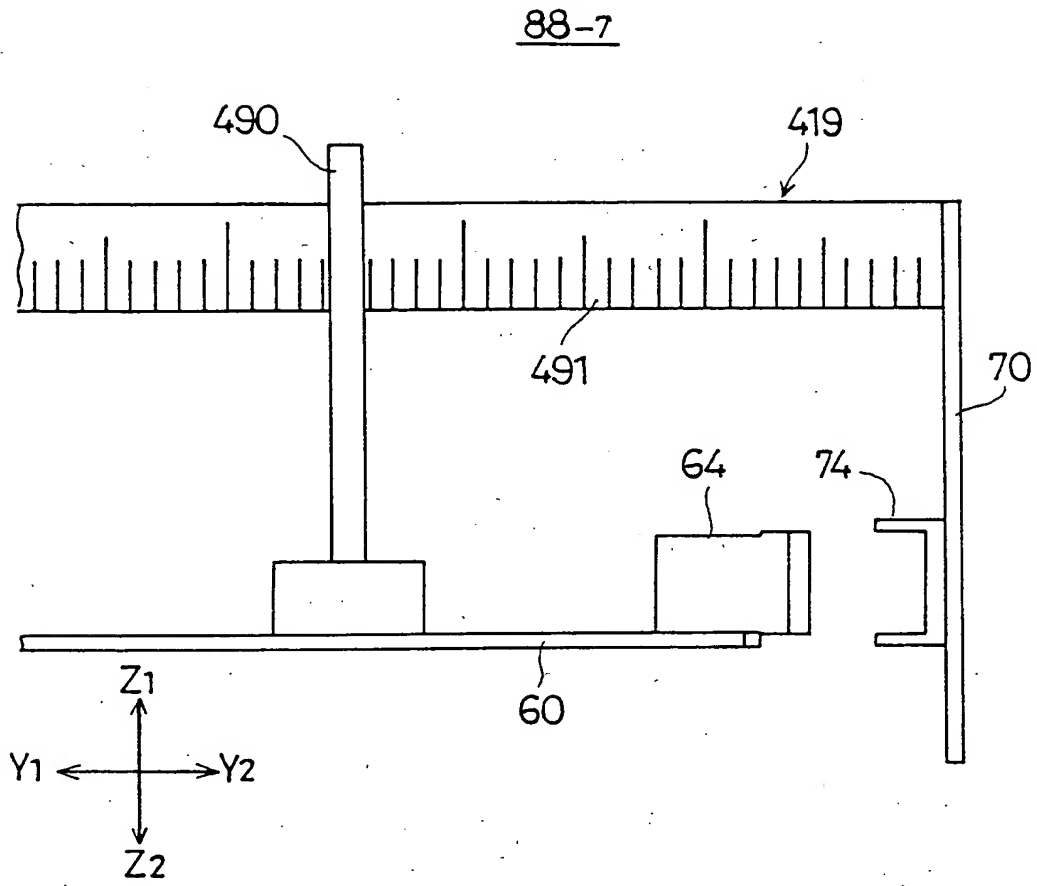


FIG. 40

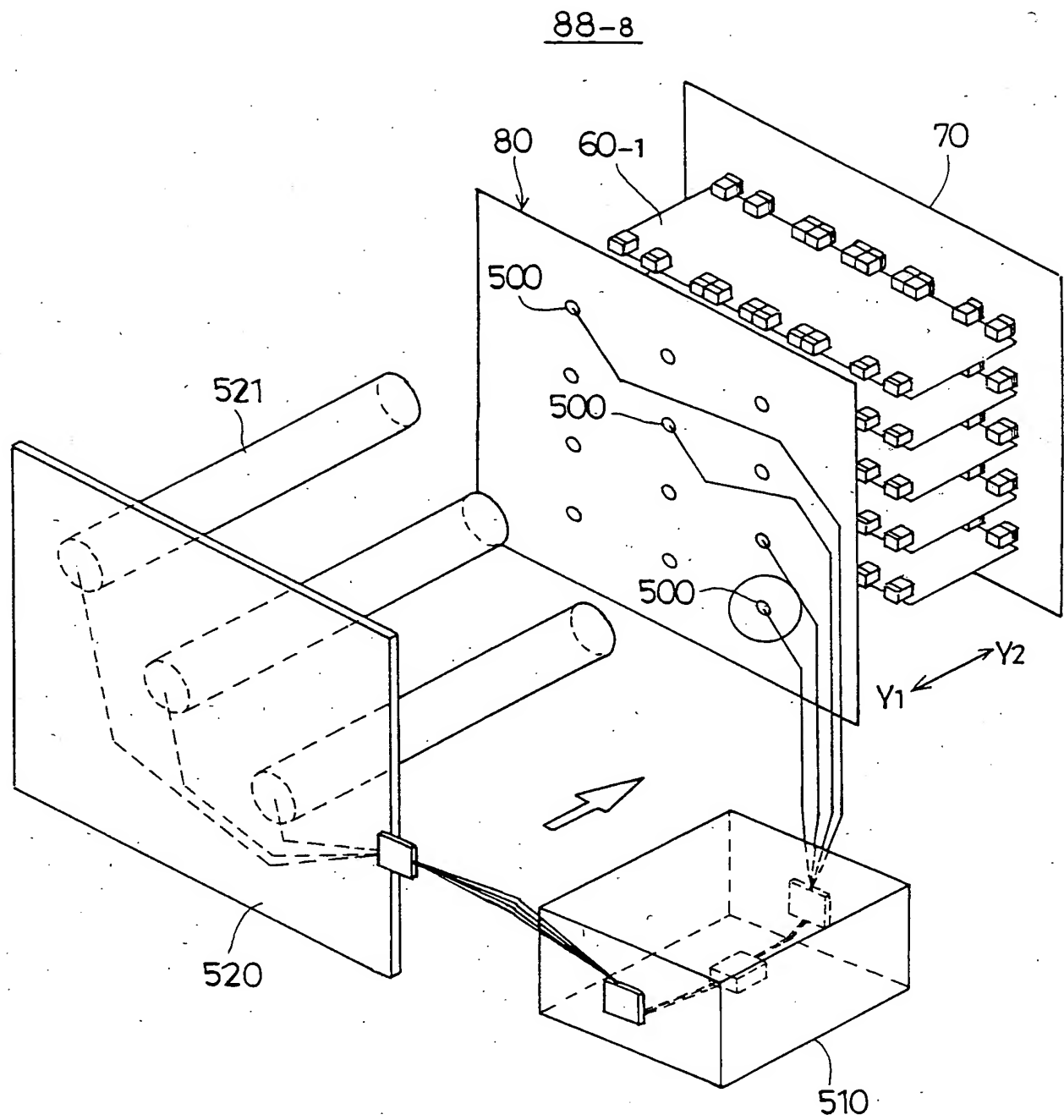




FIG. 41

